# WINBOND I/O

# W83877TF/W83877TG

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winbond

## W83877TF Datasheet Revision History

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# 1. GENERAL DESCRIPTION

W83877TF/TG is an enhanced version from Winbond's most popular I/O chip W83877F --- which integrates the disk drive adapter, serial port (UART), IrDA 1.0 SIR, parallel port, configurable Plug-and-Play registers for the whole chip --- plus additional powerful features: **ACPI** / legacy power management, **serial IRQ,** and **IRQ sharing**.

The disk drive adapter functions of W83877TF/TG include a floppy disk controller compatible with the industry standard 82077/765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, interrupt and DMA logic. The wide range of functions integrated into W83877TF/TG greatly reduces the number of components required for interfacing with floppy disk drives. W83877TF/TG supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/S, 300 Kb/S, 500 Kb/S,1 Mb/S, and 2 Mb/S.

W83877TF/TG provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. One of the UARTs support infrared (IR) IrDA1.0. Both UARTs provide legacy speed with baud rate up to 115.2K and provide advanced speed with baud rate up to **230k**, **460k**, and **921k bps** which support higher speed Modems.

W83877TF/TG supports one PC-compatible printer port (SPP), Bi-directional printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected. This function is especially valuable for notebook computer applications.

Winbond W83877TF/TG provides functions that comply with **ACPI** (Advanced Configuration and Power Interface), which includes support of legacy and ACPI power management through SMI or SCI function pins. One 24-bits power management timer is implemented with the carry notify interrupt. W83877TF/TG also has auto power management mode to reduce the power consumption.

The **serial IRQ** for PCI architecture is supported, ISA IRQs (IRQ1~IRQ15) can be cascaded into one IRQSER pin. W83877TF/TG also features ISA bus **IRQ sharing** and allows two or more devices to share the same IRQ pin.

W83877TF/TG is made to fully comply with **Microsoft™ PC97 Hardware Design Guide**. IRQs, DMAs, and I/O space resources are flexible to adjust to meet ISA PnP requirement. Moreover W83877TF/TG is made to meet the specification of PC97's requirement in the power management: **ACPI** and **DPM** (Device Power Management).

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP registers are compatible with the Plug-and-Play feature demand of Windows 95™ , which makes system resource allocation more efficient than ever.

Another benefit of W83877TF/TG is that it is pin-to-pin compatible to W83877F, and all of the 100-pin Winbond I/O IC family. Thus makes the design of applications very convenient and flexible.

## 2. FEATURES

### General:

- Plug & Play 1.0A Compliant
- Support 8 IRQs (ISA), or 15 IRQs (Serial IRQ), 3 DMA channels, and 480 re-locatable address
- Capable of ISA Bus **IRQ Sharing**
- Comply with **Microsoft PC 97** Hardware Design Guide
- Support **DPM** (Device Power Management), **ACPI**
- Report ACPI status interrupt by SCI signal from $\overline{\text{SCI}}$ pin, serial IRQ IRQSER pin, or IRQ A~H pins
- Single 24MHz/48MHZ clock input

### FDC:

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- DMA enable logic
- Supports floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signalwas forced to be inactive)
- Supports up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Supports vertical recording format
- **Support 3-mode FDD, and its Win95 driver**
- 16-byte data FIFOs

### UART:

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  - 5, 6, 7 or 8-bit characters
  - Even, odd or no parity bit generation/detection
  - 1, 1.5 or 2 stop bits generation
- Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation

- Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to ($2^{16}$-1)
- Maximum baud rate is up to 921k bps for 14.768MHz and 1.5M bps for 24MHz

**Infrared:**

- Supports IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Supports SHARP ASK-IR protocol with maximum baud rate up to 57600 bps

**Parallel Port:**

- Compatible with IBM parallel port
- Supports PS/2 compatible bi-directional parallel port
- Supports Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Supports Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

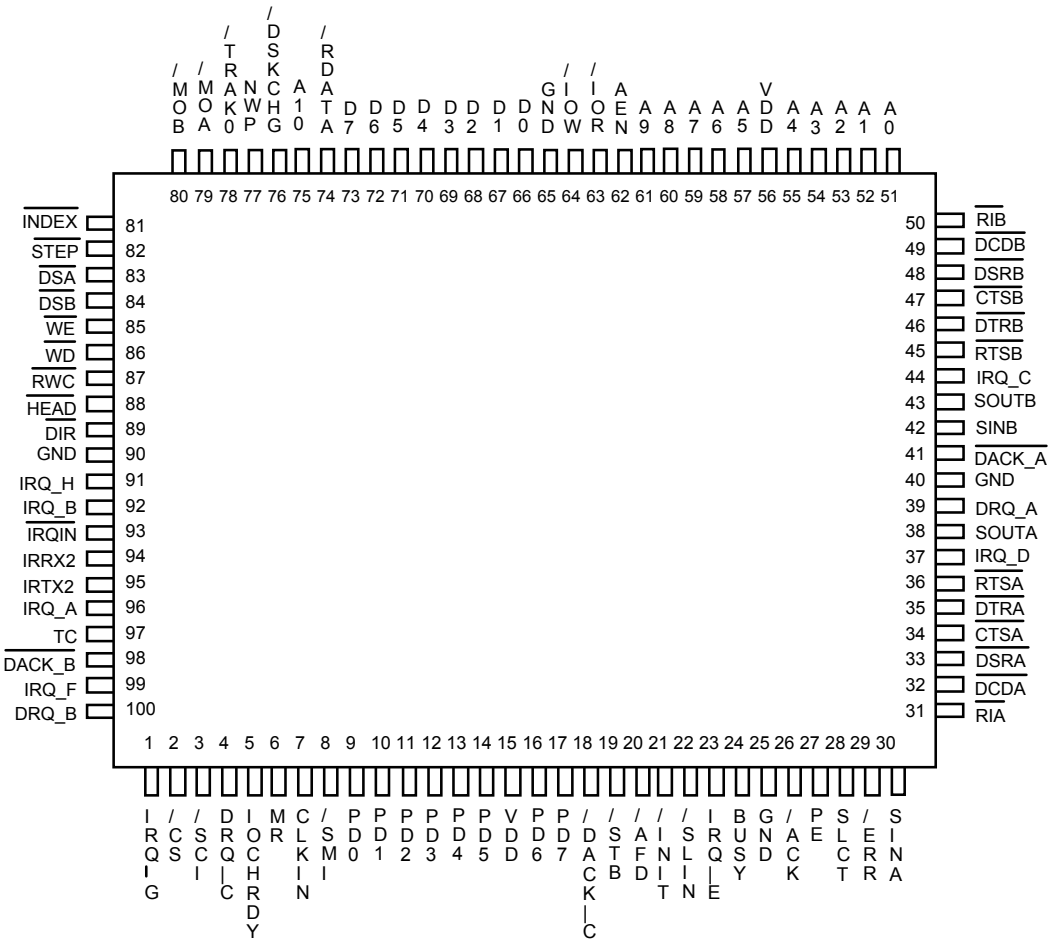
**Others:**

- Programmable configuration settings
- Immediate or automatic power-down mode for the power management
- All hardware power-on settings have internal pull-up or pull-down resistors as default value
- Dedicated Infrared Communication Pins

**Package:**

- 100-pin QFP (W83877TF/TG), and also 100-pin LQFP (W83877TD/TG)

## 3. PIN CONFIGURATION



## 4. PIN DESCRIPTION

(Note: Refer to section 12.2 DC CHARACTERISTICS for details.)

I/O8tc - TTL level output pin with 8 mA source-sink capability; CMOS level input voltage

I/O12t - TTL level bi-directional pin with 12 mA source-sink capability

I/O24t - TTL level bi-directional pin with 24 mA source-sink capability

OUT8t - TTL level output pin with 8 mA source-sink capability

OUT12t - TTL level output pin with 12 mA source-sink capability

OD12 - Open-drain output pin with 12 mA sink capability

OD24 - Open-drain output pin with 24 mA sink capability

INt - TTL level input pin

INts - TTL level Schmitt-triggered input pin

INc - CMOS level input pin

INcs - CMOS level Schmitt-triggered input pin

### 4.1 Host Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| D0–D7 | 66-73 | $I/O_{24t}$ | System data bus bits 0-7. |
| A0–A9 | 51-55<br>57-61 | $IN_t$ | System address bus bits 0-9. |
| A10 | 75 | $IN_t$ | In ECP Mode, this pin is the A10 address input. |
| IOCHRDY | 5 | $OD_{24}$ | In EPP Mode, this pin is the IO Channel Ready output to extend the host read/write cycle. |
| MR | 6 | $IN_{ts}$ | Master Reset. Active high. MR is low during normal operations. |
| $\overline{CS}$ | 2 | $IN_t$ | Active low chip select signal. |
| AEN | 62 | $IN_t$ | System address bus enable. |
| $\overline{IOR}$ | 63 | $IN_{ts}$ | CPU I/O read signal. |
| $\overline{IOW}$ | 64 | $IN_{ts}$ | CPU I/O write signal. |
| DRQ_B | 100 | $OUT_{12t}$ | DMA request signal B. |
| $\overline{DACK_B}$ | 98 | $IN_{ts}$ | DMA Acknowledge signal B. |
| DRQ_C | 4 | OUT12t | DMA request signal C. |
| $\overline{DACK_C}$ | 18 | INts | DMA Acknowledge signal C. |
| TC | 97 | INts | Terminal Count. When active, this pin indicates termination of a DMA transfer. |
| IRQIN | 93 | INt | Interrupt request input for IRQ routing ; For example , the IRQ12 can be routed into this port when PS/2 mouse is not installed. |

Host Interface, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| IRQ_A | 96 | $OUT_{12t}$ | Interrupt request signal A, when CR16 Bit 5 (G1IQSEL) = 0. |
| GIO1 | | $I/O_{12t}$ | General Purpose I/O port 1, when CR16 Bit 5 (G1IQSEL) = 1. |
| IRQ_B | 92 | $OUT_{12t}$ | Interrupt request signal B, when CR16 Bit 4 (G0IQSEL) = 0. |
| GIO0 | | $I/O_{12t}$ | General Purpose I/O port 0, when CR16 Bit 4 (G0IQSEL) = 1. |
| IRQ_C | 44 | $OUT_{12t}$ | Interrupt request signal C. |
| IRQ_D | 37 | $OUT_{12t}$ | Interrupt request signal D. |
| IRQ_E | 23 | $OUT_{12t}$ | Interrupt request signal E. |
| IRQ_F | 99 | $OUT_{12t}$ | Interrupt request signal F. |
| IRQ_G | 1 | $OUT_{12t}$ | Interrupt request signal G. |
| PCICLK | | $IN_t$ | PCI clock input, when the serial IRQ function is selected. |
| IRQ_H | 91 | $OUT_{12t}$ | Interrupt request signal H. |
| SERIRQ | | $I/O_{12t}$ | Serial interrupt input/output, when the Serial IRQ mode is selected by setting IRQMODS bit in CR31 register. |
| $\overline{SCI}$ | 3 | $OD_{12}$ | For the ACPI power management, $\overline{SCI}$ is active low 200ns for the power management events, which generate an SCI interrupt in the ACPI mode. |
| CLKIN | 7 | $IN_t$ | 24MHz/48MHZ clock input. CLKINSEL bit in CR2C register should be correctly reset/set according to the input frequency. |
| $\overline{SMI}$ | 8 | $OD_{12}$ | For the legacy power management, the $\overline{SMI}$ is active low 200ns for the power management events, which generate an SMI interrupt in the legacy power management mode.<br>This SMI output is enabled by setting the SMI_EN bit in CR3A register. |
| $\overline{DACK_A}$ | 41 | $IN_{ts}$ | DMA acknowledge signal A. |
| DRQ_A | 39 | $OUT_{12t}$ | DMA request signal A. |

## 4.2 Serial Port Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| SINA<br>SINB/IRRX1 | 30<br>42 | $IN_t$ | Serial Input. It is used to receive serial data from the communication link. |
| $\overline{RIA}$<br>$\overline{RIB}$ | 31<br>50 | $IN_t$ | Ring Indicator. An active low indicates that a ring signal is being received by the modem or data set. |
| $\overline{DCDA}$<br>$\overline{DCDB}$ | 32<br>49 | $IN_t$ | Data Carrier Detect. An active low indicates the modem or data set has detected a data carrier. |
| $\overline{DSRA}$<br>$\overline{DSRB}$ | 33<br>48 | $IN_t$ | Data Set Ready. An active low indicates the modem or data set is ready to establish a communication link and transfer data to the UART. |
| $\overline{CTSA}$ | 34 | $IN_t$ | Clear To Send. It is the modem control input. |
| $\overline{CTSB}$ | 47 | | The function of these pins can be tested by reading Bit 4 of the handshake status register. |
| $\overline{DTRA}$ | 35 | $I/O_{8tc}$ | UART A Data Terminal Ready. An active low informs the modem or data set that the controller is ready to communicate. |
| PHEFRAS | | | During power-on reset, this pin is pulled down internally and is defined as PHEFRAS, which provides the power-on value for CR16 bit 0 (HEFRAS). While it is at Low, it selects the EFER (Extended Functions Enable Register) to be 250H. While it is at High, it selects the EFER to be 3F0H. A 4.7 kΩ is recommended when intends to pull up at power-on reset. |
| $\overline{RTSA}$ | 36 | $I/O_{8tc}$ | UART A Request To Send. An active low informs the modem or data set that the controller is ready to send data. |
| PPNPCVS | | | During power-on reset, this pin is pulled up internally and is defined as PPNPCVS, which provides the power-on value for CR16 bit 2 (PNPCVS). While it is at Low, all PnP-related registers (CR20 to CR29) are all set to be 0s. While it is at High, all PnP-related registers (CR20 to CR 29) are set to default values. A 4.7 kΩ is recommended when intends to pull down at power-on reset. |
| SOUTA | 38 | $I/O_{8tc}$ | UART A Serial Output. It is used to transmit serial data out to the communication link. |
| PENFDC | | | During power-on reset, this pin is pulled up internally and used to enable or disable the FDC. While it is at Low, FDC PnP-related register (CR20) is set to be 0, i.e. FDC is disabled. While it is at High, CR20 is set to the default value, i.e. FDC is enabled. A 4.7 kΩ is recommended when intends to pull down at power-on reset. |

Serial Port Interface, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| SOUTB<br>IRTX1<br>PIRQMDS | 43 | $I/O_{8tc}$ | UART B Serial Output. It is used to transmit serial data out to the communication link.<br>During power-on reset, this pin is pulled down internally and is defined as PIRQMDS to select the IRQ mode. While it is at Low, IRQ pins can be set to Normal mode or IRQ sharing mode which decided by CR18. If it is at High, the Serial IRQ mode is selected. A 4.7 kΩ is recommended when intending to pull up at power-on reset. |
| $\overline{RTSB}$ | 45 | $I/O_{8tc}$ | UART B Request To Send. An active low informs the modem or data set that the controller is ready to send data. |
| PGOIQSEL | | | During power-on reset, this pin is pulled down internally and is defined as PGOIQSEL, which provides the power-on value for CR16 bit 4 and bit 5 (G0IQSEL & G1IQSEL). While it is at Low, pins 92 and 96 function as IRQ pins IRQ_B,IRQ_A respectively. While it is at high, pins 92 and 96 function as General Purpose I/O pins GIO0,GIO1 respectively. A 4.7 kΩ is recommended when intends to pull up at power-on reset. |
| $\overline{DTRB}$ | 46 | $I/O_{8tc}$ | UART B Data Terminal Ready. An active low informs the modem or data set that the controller is ready to communicate. |
| IRTX2 | 95 | $OUT_{12t}$ | Functions as a InfraRed data transmission line. |
| IRRX2 | 94 | $IN_t$ | Functions as a InfraRed data receiving line. |

## 4.3 Multi-Mode Parallel Port

The following pins have six functions, which are controlled by bits PRTMOD0, PRTMOD1, and PRTMOD2 of CR0 and CR9 (refer to section 11.0, Extended Functions).

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| BUSY | 24 | $IN_t$ | PRINTER MODE: BUSY<br>An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | $OD_{12}$ | EXTENSION FDD MODE: $\overline{MOB2}$<br>This pin is for Extension FDD B; the function of this pin is the same as that of the $\overline{MOB}$ pin. |
| | | $OD_{12}$ | EXTENSION 2FDD MODE: $\overline{MOB2}$<br>This pin is for Extension FDD A and B; the function of this pin is the same as that of the $\overline{MOB}$ pin. |

Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| $\overline{ACK}$ | 26 | $IN_t$ | PRINTER MODE: $\overline{ACK}$<br>An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | $OD_{12}$ | EXTENSION FDD MODE: $\overline{DSB2}$<br>This pin is for the Extension FDD B; its functions are the same as those of the $\overline{DSB}$ pin. |
| | | $OD_{12}$ | EXTENSION 2FDD MODE: $\overline{DSB2}$<br>This pin is for Extension FDD A and B; the function of this pin is the same as that of the $\overline{DSB}$ pin. |
| PE | 27 | $IN_t$ | PRINTER MODE: PE<br>An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally.<br>Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | $OD_{12}$ | EXTENSION FDD MODE: $\overline{WD2}$<br>This pin is for Extension FDD B; its function is the same as that of the $\overline{WD}$ pin. |
| | | $OD_{12}$ | EXTENSION 2FDD MODE: $\overline{WD2}$<br>This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{WD}$ pin. |
| SLCT | 28 | $IN_t$ | PRINTER MODE: SLCT<br>An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | $OD_{12}$ | EXTENSION FDD MODE: WE2<br>This pin is for Extension FDD B; its functions are the same as those of the $\overline{WE}$ pin. |
| | | $OD_{12}$ | EXTENSION 2FDD MODE: $\overline{WE2}$<br>This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{WE}$ pin. |

Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| $\overline{ERR}$ | 29 | $IN_t$ | PRINTER MODE: $\overline{ERR}$<br>An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | $OD_{12}$ | EXTENSION FDD MODE: $\overline{HEAD2}$<br>This pin is for Extension FDD B; its function is the same as that of the $\overline{HEAD}$ pin. |
| | | $OD_{12}$ | EXTENSION 2FDD MODE: $\overline{HEAD2}$<br>This pin is for Extension FDD A and B; its function is the same as that of the $\overline{HEAD}$ pin. |
| $\overline{SLIN}$ | 22 | $OD_{12}$ | PRINTER MODE: $\overline{SLIN}$<br>Output line for detection of printer selection. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | $OD_{12}$ | EXTENSION FDD MODE: $\overline{STEP2}$<br>This pin is for Extension FDD B; its function is the same as that of the $\overline{STEP}$ pin. |
| | | $OD_{12}$ | EXTENSION 2FDD MODE: $\overline{STEP2}$<br>This pin is for Extension FDD A and B; its function is the same as that of the $\overline{STEP}$ pin . |
| $\overline{INIT}$ | 21 | $OD_{12}$ | PRINTER MODE: $\overline{INIT}$<br>Output line for the printer initialization. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | $OD_{12}$ | EXTENSION FDD MODE: $\overline{DIR2}$<br>This pin is for Extension FDD B; its function is the same as that of the $\overline{DIR}$ pin. |
| | | $OD_{12}$ | EXTENSION 2FDD MODE: $\overline{DIR2}$<br>This pin is for Extension FDD A and B; its function is the same as that of the $\overline{DIR}$ pin. |

Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| $\overline{AFD}$ | 20 | OD12 | PRINTER MODE: $\overline{AFD}$<br>An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | $OD_{12}$ | EXTENSION FDD MODE: $\overline{RWC2}$<br>This pin is for Extension FDD B; its function is the same as that of the $\overline{RWC}$ pin. |
| | | $OD_{12}$ | EXTENSION 2FDD MODE: $\overline{RWC2}$<br>This pin is for Extension FDD A and B; its function is the same as that of the $\overline{RWC}$ pin. |
| $\overline{STB}$ | 19 | $OD_{12}$ | PRINTER MODE: $\overline{STB}$<br>An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | -<br>- | EXTENSION FDD MODE: NC pin<br>EXTENSION 2FDD MODE: NC pin |
| PD0 | 9 | $I/O_{24t}$ | PRINTER MODE: PD0<br>Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | $IN_t$ | EXTENSION FDD MODE: $\overline{INDEX2}$<br>This pin is for Extension FDD B; the function of this pin is the same as that of the $\overline{INDEX}$ pin. This pin is pulled high internally. |
| | | $IN_t$ | EXTENSION 2FDD MODE: $\overline{INDEX2}$<br>This pin is for Extension FDD A and B; this function of this pin is the same as $\overline{INDEX}$ pin. This pin is pulled high internally. |
| PD1 | 10 | I/O24t | PRINTER MODE: PD1<br>Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | INt | EXTENSION FDD MODE: $\overline{TRAK02}$<br>This pin is for Extension FDD B; the function of this pin is the same as that of the $\overline{TRAK0}$ pin. This pin is pulled high internally. |
| | | INt | EXTENSION. 2FDD MODE: $\overline{TRAK02}$<br>This pin is for Extension FDD A and B; this function of this pin is the same as $\overline{TRAK0}$ pin. This pin is pulled high internally. |

Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| PD2 | 11 | I/O24t | PRINTER MODE: PD2<br>Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | $IN_t$ | EXTENSION FDD MODE: $\overline{WP2}$<br>This pin is for Extension FDD B; the function of this pin is the same as that of the $\overline{WP}$ pin. This pin is pulled high internally. |
| | | $IN_t$ | EXTENSION. 2FDD MODE: $\overline{WP2}$<br>This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{WP}$ pin. This pin is pulled high internally. |
| PD3 | 12 | $I/O_{24t}$ | PRINTER MODE: PD3<br>Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | $IN_t$ | EXTENSION FDD MODE: $\overline{RDATA2}$<br>Motor on B for Extension FDD B; the function of this pin is the same as that of the $\overline{RDATA}$ pin. This pin is pulled high internally. |
| | | $IN_t$ | EXTENSION 2FDD MODE: $\overline{RDATA2}$<br>This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{RDATA}$ pin. This pin is pulled high internally. |
| PD4 | 13 | I/O24t | PRINTER MODE: PD4<br>Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | INt | EXTENSION FDD MODE: $\overline{DSKCHG2}$<br>Drive select B for Extension FDD B; the function of this pin is the same as that of $\overline{DSKCHG}$ pin. This pin is pulled high internally. |
| | | INt | EXTENSION 2FDD MODE: $\overline{DSKCHG2}$<br>This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{DSKCHG}$ pin. This pin is pulled high internally. |
| PD5 | 14 | I/O24t<br><br><br><br>I/O24t<br>I/O24t | PRINTER MODE: PD5<br>Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.<br>EXTENSION FDD MODE: This pin is a tri-state output.<br>EXTENSION 2FDD MODE: This pin is a tri-state output. |

Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| PD6 | 16 | $I/O_{24t}$ | PRINTER MODE: PD6<br>Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | - | EXTENSION FDD MODE: NC pin |
| | | $OD_{24}$ | EXTENSION. 2FDD MODE: $\overline{MOA2}$<br>This pin is for Extension FDD A; its function is the same as that of the $\overline{MOA}$ pin. |
| PD7 | 17 | $I/O_{24t}$ | PRINTER MODE: PD7<br>Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | - | EXTENSION FDD MODE: NC pin |
| | | $OD_{24}$ | EXTENSION 2FDD MODE: $\overline{DSA2}$<br>This pin is for Extension FDD A; its function is the same as that of the $\overline{DSA}$ pin. |

## 4.4 FDC Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| $\overline{WE}$ | 85 | $OD_{24}$ | Write enable. An open drain output. |
| $\overline{DIR}$ | 89 | $OD_{24}$ | Direction of the head step motor. An open drain output.<br>Logic 1 = outward motion<br>Logic 0 = inward motion |
| $\overline{HEAD}$ | 88 | $OD_{24}$ | Head select. This open drain output determines which disk drive head is active.<br>Logic 1 = side 0<br>Logic 0 = side 1 |
| $\overline{RWC}$ | 87 | $OD_{24}$ | Reduced write current. This signal can be used on two-speed disk drives to select the transfer rate. An open drain output.<br>Logic 0 = 250 Kb/s<br>Logic 1 = 500 Kb/s<br>When bit 5 of CR9 (EN3MODE) is set to high, the three-mode FDD function is enabled, and the pin will have a different definition. Refer to the EN3MODE bit in CR9. |
| $\overline{WD}$ | 86 | $OD_{24}$ | Write data. This logic low open drain writes precompensation serial data to the selected FDD. An open drain output. |
| $\overline{STEP}$ | 82 | $OD_{24}$ | Step output pulses. This active low open drain output produces a pulse to move the head to another track. |

FDC Interface, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| $\overline{\text{INDEX}}$ | 81 | $IN_{cs}$ | This schmitt input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| $\overline{\text{TRAK0}}$ | 78 | $IN_{cs}$ | Track 0. This schmitt input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| $\overline{\text{WP}}$ | 77 | $IN_{cs}$ | Write protected. This active low schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| $\overline{\text{RDATA}}$ | 74 | $IN_{cs}$ | The read data input signal from the FDD. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| $\overline{\text{DSKCHG}}$ | 76 | $IN_{cs}$ | Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| $\overline{\text{MOA}}$ | 79 | $OD_{24}$ | Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output. |
| $\overline{\text{MOB}}$ | 80 | $OD_{24}$ | Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output. |
| $\overline{\text{DSA}}$ | 83 | $OD_{24}$ | Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output. |
| $\overline{\text{DSB}}$ | 84 | $OD_{24}$ | Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output. |
| VDD | 15, 56 | | +5 power supply for the digital circuitry. |
| GND | 25, 40 65, 90 | | Ground. |

# 5. FDC FUNCTIONAL DESCRIPTION

## 5.1 W83877TF/TG FDC

The floppy disk controller of W83877TF/TG integrates all of the logic required for floppy disk control. The FDC implements a PC/AT or PS/2 solution. All programmable options default to compatible values. The FIFO provides better system performance in multi-master systems. The digital data separator supports up to data rate 1 M bits/sec. (2 M bits/sec for fast tape drive)

The FDC includes the following blocks: AT interface, Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core.

### 5.1.1 AT interface

The interface consists of the standard asynchronous signals: $\overline{RD}$, $\overline{WR}$, A0-A3, IRQ, DMA control, and a data bus. The address lines select between the configuration registers, the FIFO and control/status registers. This interface can be switched between PC/AT, Model 30, or PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC/AT.

### 5.1.2 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the CONFIGURE command. The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk errors. The following tables give several examples of the delays with a FIFO. The data are based upon the following formula:

THRESHOLD × (1/Data Rate) *8 - 1.5 μS = DELAY

| FIFO THRESHOLD | MAXIMUM DELAY TO SERVICING AT 500K BPS |
|---|---|
| | Data Rate |
| 1 Byte | 1 × 16 μS - 1.5 μS = 14.5 μS |
| 2 Byte | 2 × 16 μS - 1.5 μS = 30.5 μS |
| 8 Byte | 8 × 16 μS - 1.5 μS = 6.5 μS |
| 15 Byte | 15 × 16 μS - 1.5 μS = 238.5 μS |
| **FIFO THRESHOLD** | **MAXIMUM DELAY TO SERVICING AT 1M BPS** |
| | Data Rate |
| 1 Byte | 1 × 8 μS - 1.5 μS = 6.5 μS |
| 2 Byte | 2 × 8 μS - 1.5 μS = 14.5 μS |
| 8 Byte | 8 × 8 μS - 1.5 μS = 62.5 μS |
| 15 Byte | 15 × 8 μS - 1.5 μS = 118.5 μS |

At the start of a command the FIFO is always disabled and command parameters must be sent based upon the RQM and DIO bit settings in the main status register. When the FDC enters the command execution phase, it clears the FIFO of any data to ensure that invalid data are not transferred.

An overrun and underrun will terminate the current command and the data transfer. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled with the SPECIFY command and are initiated by the FDC by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting $\overline{\text{DACK}}$ and addresses need not be valid.

Note that if the DMA controller is programmed to function in verify mode a pseudo read is performed by the FDC based only on $\overline{\text{DACK}}$. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read. With the FIFO enabled the above operation is performed by using the new VERIFY command. No DMA operation is needed.

### 5.1.3 Data Separator

The function of the data separator is to lock onto the incoming serial read data. When a lock is achieved the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The DDS circuit cycles once every 12 clock cycles ideally. Any data pulse input will be synchronized and then adjusted by immediate error adjustment. The control logic will generate RDD and RWD for every pulse input. During any cycle where no data pulse is present, the DDS cycles are based on speed. A digital integrator is used to keep track of the speed changes in the input data stream.

### 5.1.4 Write Precompensation

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and is dependent on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late relative to the surrounding bits.

### 5.1.5 Perpendicular Recording Mode

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5" floppy disks and can read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. The perpendicular mode requires a 1 Mbps data rate for the FDC. At this data rate the FIFO eases the host interface bottleneck due to the speed of data transfer to or from the disk.

### 5.1.6 Tape Drive

The W83877TF/TG supports standard tape drives (1 Mbps, 500 Kbps, 250 Kbps) and new fast tape drive (2M bps).

### 5.1.7 FDC Core

The W83877TF/TG FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor. The result can also be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information is provided to the microprocessor.

### 5.1.8 FDC Commands

Command Symbol Descriptions:

C: Cylinder number 0 - 256
D: Data Pattern
DIR: Step Direction
DIR = 0, step out
DIR = 1, step in
DS0: Disk Drive Select 0
DS1: Disk Drive Select 1
DTL: Data Length
EC: Enable Count
EOT: End of Track
EFIFO: Enable FIFO
EIS: Enable Implied Seek
EOT: End of track
FIFOTHR: FIFO Threshold
GAP: Gap length selection
GPL: Gap Length
H: Head number
HDS: Head number select
HLT: Head Load Time
HUT: Head Unload Time
LOCK: Lock EFIFO, FIFOTHR, PTRTRK bits prevent affected by software reset
MFM: MFM or FM Mode

MT: Multitrack
N: The number of data bytes written in a sector
NCN: New Cylinder Number
ND: Non-DMA Mode
OW: Overwritten
PCN: Present Cylinder Number
POLL: Polling Disable
PRETRK: Precompensation Start Track Number
R: Record
RCN: Relative Cylinder Number
R/W: Read/Write
SC: Sector/per cylinder
SK: Skip deleted data address mark
SRT: Step Rate Time
ST0: Status Register 0
ST1: Status Register 1
ST2: Status Register 2
ST3: Status Register 3
WG: Write gate alters timing of WE

### 5.1.9 FDC Instruction Sets

**(1) Read Data**

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | MT | MFM | SK | 0 | 0 | 1 | 1 | 0 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W<br>W | ---------- C ----------<br>---------- H ---------- | | | | | | | | Sector ID information prior to command execution |
| | W<br>W | ---------- R ----------<br>---------- N ---------- | | | | | | | | |
| | W<br>W | ---------- EOT ----------<br>---------- GPL ---------- | | | | | | | | |
| | W | ---------- DTL ---------- | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system |
| Result | R<br>R<br>R | ---------- ST0 ----------<br>---------- ST1 ----------<br>---------- ST2 ---------- | | | | | | | | Status information after command execution |
| | R<br>R<br>R<br>R | ---------- C ----------<br>---------- H ----------<br>---------- R ----------<br>---------- N ---------- | | | | | | | | Sector ID information after command execution |

**(2) Read Deleted Data**

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | MT | MFM | SK | 0 | 1 | 1 | 0 | 0 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ---------- C ---------- | | | | | | | | Sector ID information prior to command execution |
| | W | ---------- H ---------- | | | | | | | | |
| | W | ---------- R ---------- | | | | | | | | |
| | W | ---------- N ---------- | | | | | | | | |
| | W | ---------- EOT ---------- | | | | | | | | |
| | W | ---------- GPL ---------- | | | | | | | | |
| | W | ---------- DTL ---------- | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system |
| Result | R | ---------- ST0 ---------- | | | | | | | | Status information after command execution |
| | R | ---------- ST1 ---------- | | | | | | | | |
| | R | ---------- ST2 ---------- | | | | | | | | |
| | R | ---------- C ---------- | | | | | | | | Sector ID information after command execution |
| | R | ---------- H ---------- | | | | | | | | |
| | R | ---------- R ---------- | | | | | | | | |
| | R | ---------- N ---------- | | | | | | | | |

### (3) Read A Track

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | 0 | MFM | 0 | 0 | 0 | 0 | 1 | 0 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ---------- C ---------- | | | | | | | | Sector ID information prior to command execution |
| | W | ---------- H ---------- | | | | | | | | |
| | W | ---------- R ---------- | | | | | | | | |
| | W | ---------- N ---------- | | | | | | | | |
| | W | ---------- EOT ---------- | | | | | | | | |
| | W | ---------- GPL ---------- | | | | | | | | |
| | W | ---------- DTL ---------- | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT |
| Result | R | ---------- ST0 ---------- | | | | | | | | Status information after command execution |
| | R | ---------- ST1 ---------- | | | | | | | | |
| | R | ---------- ST2 ---------- | | | | | | | | |
| | R | ---------- C ---------- | | | | | | | | Sector ID information after command execution |
| | R | ---------- H ---------- | | | | | | | | |
| | R | ---------- R ---------- | | | | | | | | |
| | R | ---------- N ---------- | | | | | | | | |

### (4) Read ID

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | 0 | MFM | 0 | 0 | 1 | 0 | 1 | 0 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| Execution | | | | | | | | | | The first correct ID information on the cylinder is stored in Data Register |
| Result | R | ---------- ST0 ---------- | | | | | | | | Status information after command execution |
| | R | ---------- ST1 ---------- | | | | | | | | |
| | R | ---------- ST2 ---------- | | | | | | | | |
| | R | ---------- C ---------- | | | | | | | | Disk status after the command has been completed |
| | R | ---------- H ---------- | | | | | | | | |
| | R | ---------- R ---------- | | | | | | | | |
| | R | ---------- N ---------- | | | | | | | | |

**(5) Verify**

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | MT | MFM | SK | 1 | 0 | 1 | 1 | 0 | Command codes |
| | W | EC | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ---------- C ---------- | | | | | | | | Sector ID information prior to command execution |
| | W | ---------- H ---------- | | | | | | | | |
| | W | ---------- R ---------- | | | | | | | | |
| | W | ---------- N ---------- | | | | | | | | |
| | W | ---------- EOT ---------- | | | | | | | | |
| | W | ---------- GPL ---------- | | | | | | | | |
| | | ---------- DTL/SC ---------- | | | | | | | | |
| Execution | | | | | | | | | | No data transfer takes place |
| Result | R | ---------- ST0 ---------- | | | | | | | | Status information after command execution |
| | R | ---------- ST1 ---------- | | | | | | | | |
| | R | ---------- ST2 ---------- | | | | | | | | |
| | R | ---------- C ---------- | | | | | | | | Sector ID information after command execution |
| | R | ---------- H ---------- | | | | | | | | |
| | R | ---------- R ---------- | | | | | | | | |
| | R | ---------- N ---------- | | | | | | | | |

**(6) Version**

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Command codes |
| Result | W | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Enhanced controller |

**(7) Write Data**

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | MT | MFM | 0 | 0 | 0 | 1 | 0 | 1 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ---------- C ---------- | | | | | | | | Sector ID information prior to Command execution |
| | W | ---------- H ---------- | | | | | | | | |
| | W | ---------- R ---------- | | | | | | | | |
| | W | ---------- N ---------- | | | | | | | | |
| | W | ---------- EOT ---------- | | | | | | | | |
| | W | ---------- GPL ---------- | | | | | | | | |
| | W | ---------- DTL ---------- | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system |
| Result | R | ---------- ST0 ---------- | | | | | | | | Status information after Command execution |
| | R | ---------- ST1 ---------- | | | | | | | | |
| | R | ---------- ST2 ---------- | | | | | | | | |
| | R | ---------- C ---------- | | | | | | | | Sector ID information after Command execution |
| | R | ---------- H ---------- | | | | | | | | |
| | R | ---------- R ---------- | | | | | | | | |
| | R | ---------- N ---------- | | | | | | | | |

**(8) Write Deleted Data**

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | MT | MFM | 0 | 0 | 1 | 0 | 0 | 1 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ---------- C ---------- | | | | | | | | Sector ID information prior to command execution |
| | W | ---------- H ---------- | | | | | | | | |
| | W | ---------- R ---------- | | | | | | | | |
| | W | ---------- N ---------- | | | | | | | | |
| | W | ---------- EOT ---------- | | | | | | | | |
| | W | ---------- GPL ---------- | | | | | | | | |
| | W | ---------- DTL ---------- | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system |
| Result | R | ---------- ST0 ---------- | | | | | | | | Status information after command execution |
| | R | ---------- ST1 ---------- | | | | | | | | |
| | R | ---------- ST2 ---------- | | | | | | | | |
| | R | ---------- C ---------- | | | | | | | | Sector ID information after command execution |
| | R | ---------- H ---------- | | | | | | | | |
| | R | ---------- R ---------- | | | | | | | | |
| | R | ---------- N ---------- | | | | | | | | |

### (9) Format A Track

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | 0 | MFM | 0 | 0 | 1 | 1 | 0 | 1 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ---------- N ---------- | | | | | | | | Bytes/Sector |
| | W | ---------- SC ---------- | | | | | | | | Sectors/Cylinder |
| | W | ---------- GPL ---------- | | | | | | | | Gap 3 |
| | W | ---------- D ---------- | | | | | | | | Filler Byte |
| Execution for Each Sector Repeat: | W | ---------- C ---------- | | | | | | | | Input Sector Parameters |
| | W | ---------- H ---------- | | | | | | | | |
| | W | ---------- R ---------- | | | | | | | | |
| | W | ---------- N ---------- | | | | | | | | |
| Result | R | ---------- ST0 ---------- | | | | | | | | Status information after command execution |
| | R | ---------- ST1 ---------- | | | | | | | | |
| | R | ---------- ST2 ---------- | | | | | | | | |
| | R | ---------- Undefined ---------- | | | | | | | | |
| | R | ---------- Undefined ---------- | | | | | | | | |
| | R | ---------- Undefined ---------- | | | | | | | | |
| | R | ---------- Undefined ---------- | | | | | | | | |

### (10) Recalibrate

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | 0 | DS1 | DS0 | |
| Execution | | | | | | | | | | Head retracted to Track 0 Interrupt |

### (11) Sense Interrupt Status

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Command codes |
| Result | R | ---------- ST0 ---------- | | | | | | | | Status information at the end of each seek operation |
| | R | ---------- PCN ---------- | | | | | | | | |

### (12) Specify

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Command codes |
| | W | \| ---------SRT ---------- \| --------- HUT ---------- \| | | | | | | | | |
| | W | \|---------- HLT ----------\| ND | | | | | | | | |

### (13) Seek

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ---------- NCN ---------- | | | | | | | | |
| Execution | R | | | | | | | | | Head positioned over proper cylinder on diskette |

### (14) Configure

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | Configure information |
| | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | W | 0 EIS EFIFO POLL \| ------ FIFOTHR ----\| | | | | | | | | |
| | W | \| ----------PRETRK ---------- \| | | | | | | | | |
| Execution | | | | | | | | | | Internal registers written |

### (15) Relative Seek

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | 1 | DIR | 0 | 0 | 1 | 1 | 1 | 1 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | \| ---------- RCN ---------- \| | | | | | | | | |

**(16) Dumpreg**

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | Registers placed in FIFO |
| Result | R | ---------- PCN-Drive 0---------- | | | | | | | | |
| | R | ---------- PCN-Drive 1 ---------- | | | | | | | | |
| | R | ---------- PCN-Drive 2---------- | | | | | | | | |
| | R | ---------- PCN-Drive 3 ---------- | | | | | | | | |
| | R | -------- SRT ---------- \| -------- HUT ---------- | | | | | | | | |
| | R | ---------- HLT ----------\| ND | | | | | | | | |
| | R | ---------- SC/EOT ---------- | | | | | | | | |
| | R | LOCK | 0 | D3 | D2 | D1 | D0 | GAP | WG | |
| | R | 0 | EIS | EFIFO | POLL\| | --- FIFOTHR ---- \| | | | | |
| | R | ----------PRETRK ---------- | | | | | | | | |

**(17) Perpendicular Mode**

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | Command code |
| | W | OW | 0 | D3 | D2 | D1 | D0 | GAP | WG | |

**(18) Lock**

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | LOCK | 0 | 0 | 1 | 0 | 1 | 0 | 0 | Command code |
| Result | R | 0 | 0 | 0 | LOCK | 0 | 0 | 0 | 0 | |

**(19) Sense Drive Status**

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Command code |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| Result | R | ---------- ST3 ---------- | | | | | | | | Status information about disk drive |

**(20) Invalid**

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| Command | W | ---------- Invalid Codes ---------- | | | | | | | | Invalid codes (no operation - FDC goes into standby state) |
| Result | R | ---------- ST0 ---------- | | | | | | | | ST0 = 80H |

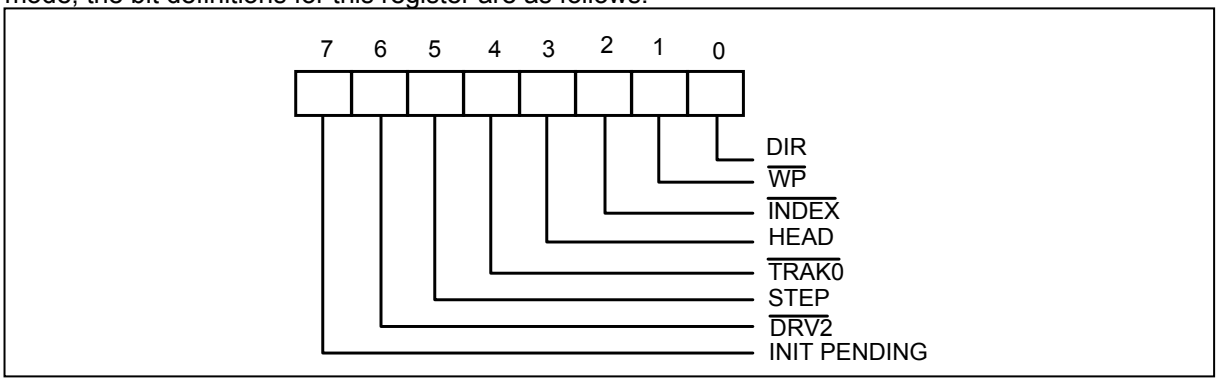
## 5.2 Register Descriptions

There are several status, data, and control registers in W83877TF/TG. These registers are defined below:

| ADDRESS | REGISTER | |
|---|---|---|
| OFFSET | READ | WRITE |
| base address + 0 | SA REGISTER | |
| base address + 1 | SB REGISTER | |
| base address + 2 | | DO REGISTER |
| base address + 3 | TD REGISTER | TD REGISTER |
| base address + 4 | MS REGISTER | DR REGISTER |
| base address + 5 | DT (FIFO) REGISTER | DT (FIFO) REGISTER |
| base address + 7 | DI REGISTER | CC REGISTER |

### 5.2.1 Status Register A (SA Register) (Read base address + 0)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:




INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

DRV2 (Bit 6):

0 A second drive has been installed

1 A second drive has not been installed

STEP (Bit 5):

This bit indicates the complement of STEP output.

TRAK0 (Bit 4):

This bit indicates the value of TRAK0 input.

HEAD (Bit 3):

This bit indicates the complement of HEAD output.

0 side 0

1 side 1

$\overline{\text{INDEX}}$ (Bit 2):

This bit indicates the value of $\overline{\text{INDEX}}$ output.

$\overline{\text{WP}}$ (Bit 1):

0 disk is write-protected

1 disk is not write-protected

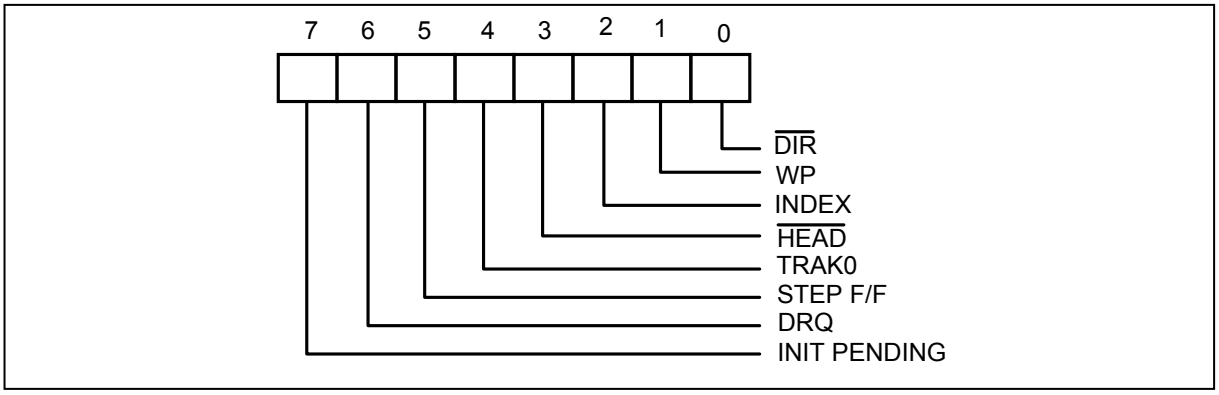
DIR (Bit 0)

This bit indicates the direction of head movement.

0 outward direction

1 inward direction

In PS/2 Model 30 mode, the bit definitions for this register are as follows:




INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

DRQ (Bit 6):

This bit indicates the value of DRQ output pin.

STEP F/F (Bit 5):

This bit indicates the complement of latched $\overline{\text{STEP}}$ output.

TRAK0 (Bit 4):

This bit indicates the complement of $\overline{\text{TRAK0}}$ input.

$\overline{\text{HEAD}}$ (Bit 3):

This bit indicates the value of $\overline{\text{HEAD}}$ output.

0 side 1

1 side 0

INDEX (Bit 2):

This bit indicates the complement of $\overline{\text{INDEX}}$ output.

WP (Bit 1):

0 disk is not write-protected

1 disk is write-protected

$\overline{\text{DIR}}$ (Bit 0)

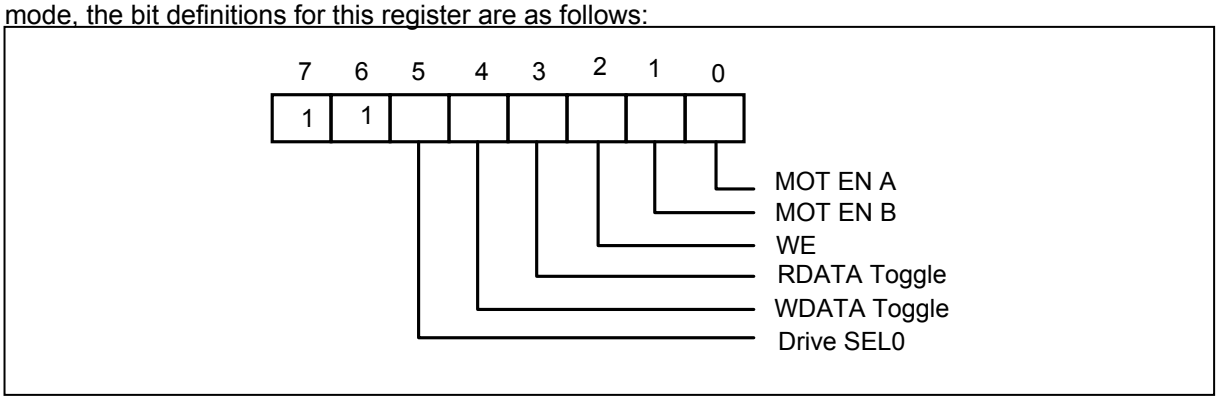
This bit indicates the direction of head movement.

0 inward direction

1 outward direction

### 5.2.2 Status Register B (SB Register) (Read base address + 1)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:




Drive SEL0 (Bit 5):

This bit indicates the status of DO REGISTER bit 0 (drive select bit 0).

WDATA Toggle (Bit 4):

This bit changes state at every rising edge of the $\overline{\text{WD}}$ output pin.

RDATA Toggle (Bit 3):

This bit changes state at every rising edge of the $\overline{\text{RDATA}}$ output pin.

WE (Bit 2):

This bit indicates the complement of the $\overline{\text{WE}}$ output pin.

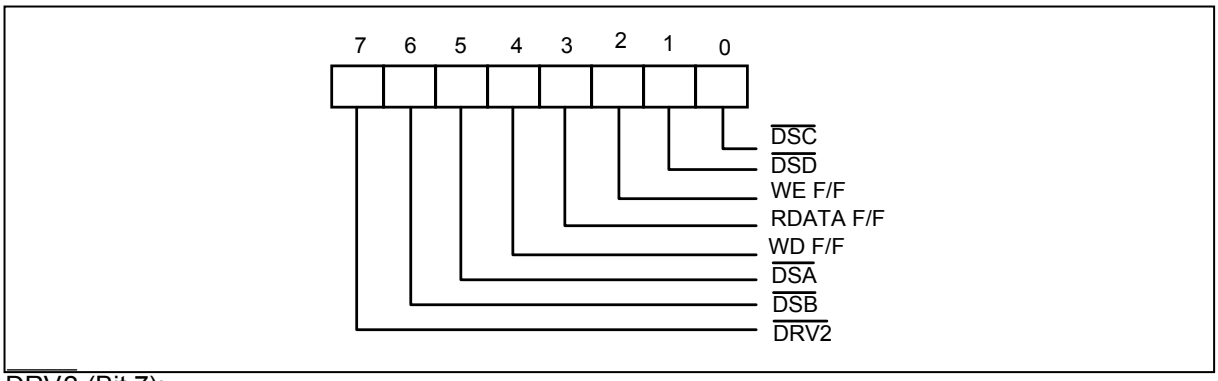
MOT EN B (Bit 1)

This bit indicates the complement of the $\overline{\text{MOB}}$ output pin.

MOT EN A (Bit 0)

This bit indicates the complement of the $\overline{\text{MOA}}$ output pin.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:




DRV2 (Bit 7):

0 A second drive has been installed

1 A second drive has not been installed

DSB (Bit 6):

This bit indicates the status of DSB output pin.

DSA (Bit 5):

This bit indicates the status of DSA output pin.

WD F/F(Bit 4):

This bit indicates the complement of the latched WD output pin at every rising edge of the WD output pin.

RDATA F/F(Bit 3):

This bit indicates the complement of the latched RDATA output pin .

WE F/F (Bit 2):

This bit indicates the complement of latched WE output pin.

DSD (Bit 1):

0 Drive D has been selected

1 Drive D has not been selected

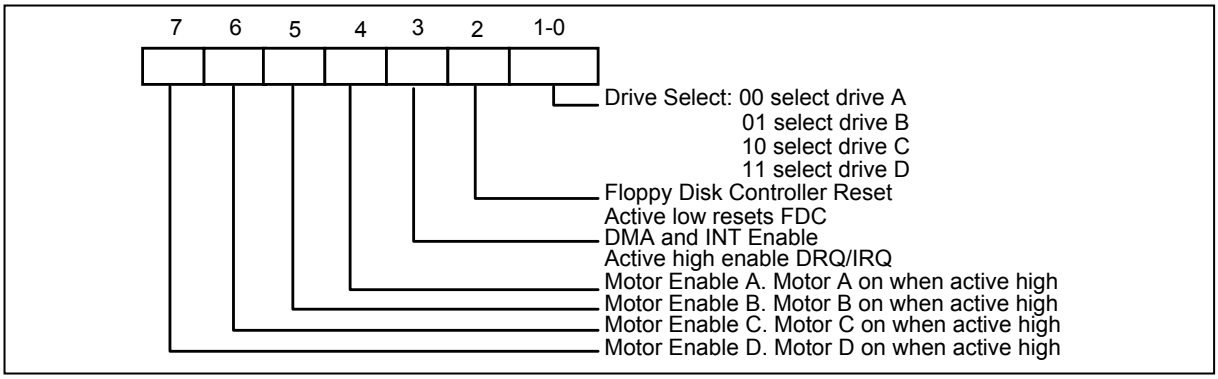
DSC (Bit 0):

0 Drive C has been selected

1 Drive C has not been selected

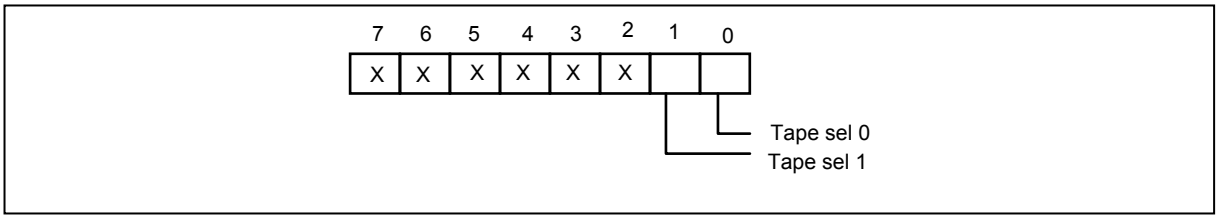
### 5.2.3 Digital Output Register (DO Register) (Write base address + 2)

The Digital Output Register is a write-only register controlling drive motors, drive selection, DRQ/IRQ enable, and FDC resetting. All the bits in this register are cleared by the MR pin. The bit definitions are as follows:

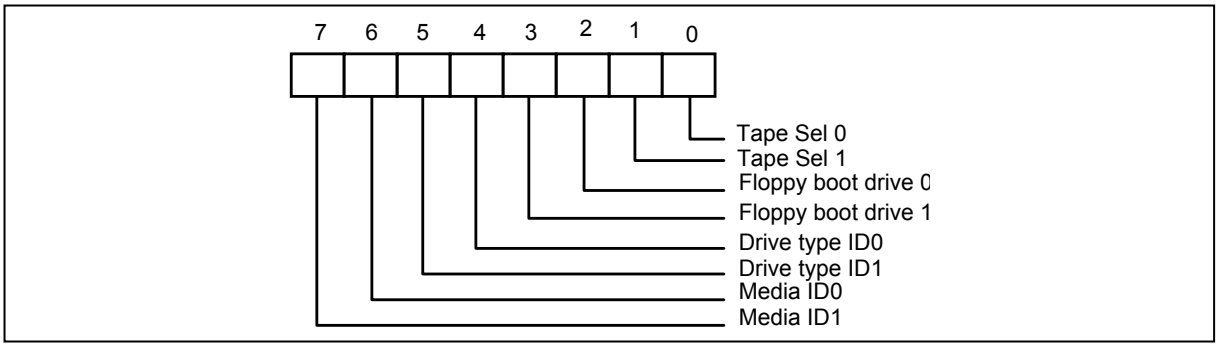



### 5.2.4 Tape Drive Register (TD Register) (Read base address + 3)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information of the floppy disk drive. In normal floppy mode, this register includes only bit 0 and 1. The bit definitions are as follows:




If three mode FDD function is enabled (EN3MODE = 1 in CR9), the bit definitions are as follows:




Media ID1 Media ID0 (Bit 7, 6):

These two bits are read only. These two bits reflect the value of CR8 bit 3, 2.

Drive type ID1 Drive type ID0 (Bit 5, 4):

These two bits reflect two of the bits of CR7. Which two bits are reflected depends on the last drive selected in the DO REGISTER.

Floppy Boot drive 1, 0 (Bit 3, 2):

These two bits reflect the value of CR8 bit 1, 0.

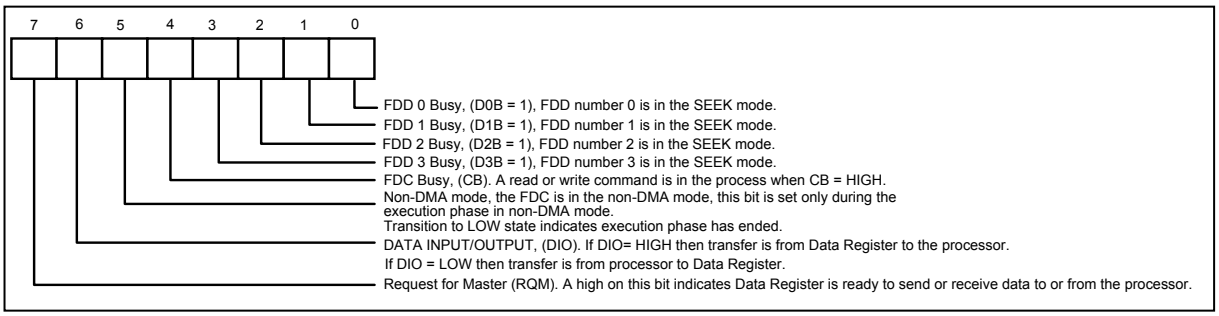
Tape Sel 1, Tape Sel 0 (Bit 1, 0):

These two bits assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved as the floppy disk boot drive.

| TAPE SEL 1 | TAPE SEL 0 | DRIVE SELECTED |
|---|---|---|
| 0 | 0 | None |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

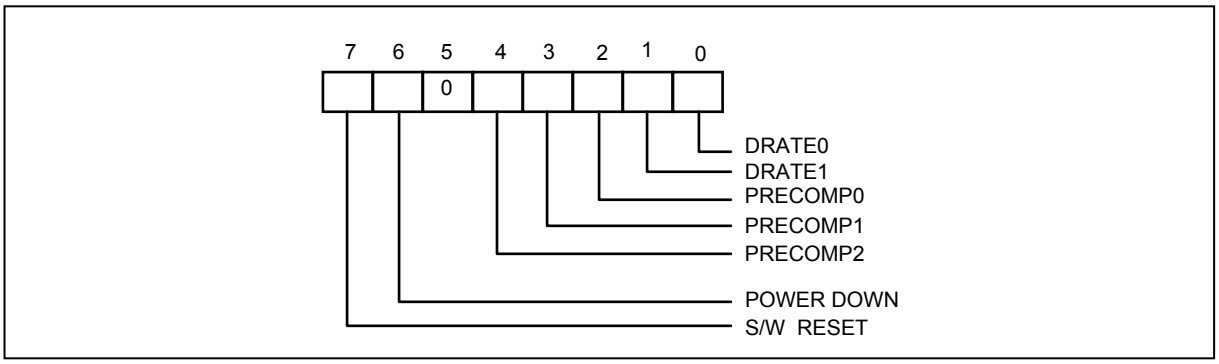
### 5.2.5 Main Status Register (MS Register) (Read base address + 4)

The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:




### 5.2.6 Data Rate Register (DR Register) (Write base address + 4)

The Data Rate Register is used to set the transfer rate and write precompensation. The data rate of the FDC is programmed by the CC REGISTER for PC-AT and PS/2 Model 30 and PS/2 mode, and not by the DR REGISTER. The real data rate is determined by the most recent write to either of the DR REGISTER or CC REGISTER.



S/W RESET (Bit 7):

This bit is the software reset bit.

POWER-DOWN (Bit 6):

0 FDC in normal mode

1 FDC in power-down mode

PRECOMP2 PRECOMP1 PRECOMP0 (Bit 4, 3, 2):

These three bits select the value of write precompensation. The following tables show the precompensation values for the combination of these bits.

| PRECOM | PRECOMPENSATION DELAY | |
|---|---|---|
| **2 1 0** | 250K - 1Mbps | 2 Mbps Tape drive |
| 0 0 0 | Default Delays | Default Delays |
| 0 0 1 | 41.67 nS | 20.8nS |
| 0 1 0 | 83.34 nS | 41.17nS |
| 0 1 1 | 125.00 nS | 62.5nS |
| 1 0 0 | 166.67 nS | 83.3nS |
| 1 0 1 | 208.33 nS | 104.2nS |
| 1 1 0 | 250.00 nS | 125.00nS |
| 1 1 1 | 0.00 nS (disabled) | 0.00nS (disabled) |

| DATA RATE | DEFAULT PRECOMPENSATION DELAYS |
|---|---|
| 250 KB/S | 125 nS |
| 300 KB/S | 125 nS |
| 500 KB/S | 125 nS |
| 1 MB/S | 41.67 nS |
| 2 MB/S | 20.8 nS |

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC and reduced write current control.

00 500 KB/S (MFM), 250 KB/S (FM), $\overline{RWC}$ = 1.

01 300 KB/S (MFM), 150 KB/S (FM), $\overline{RWC}$ = 0.

10 250 KB/S (MFM), 125 KB/S (FM), $\overline{RWC}$ = 0.

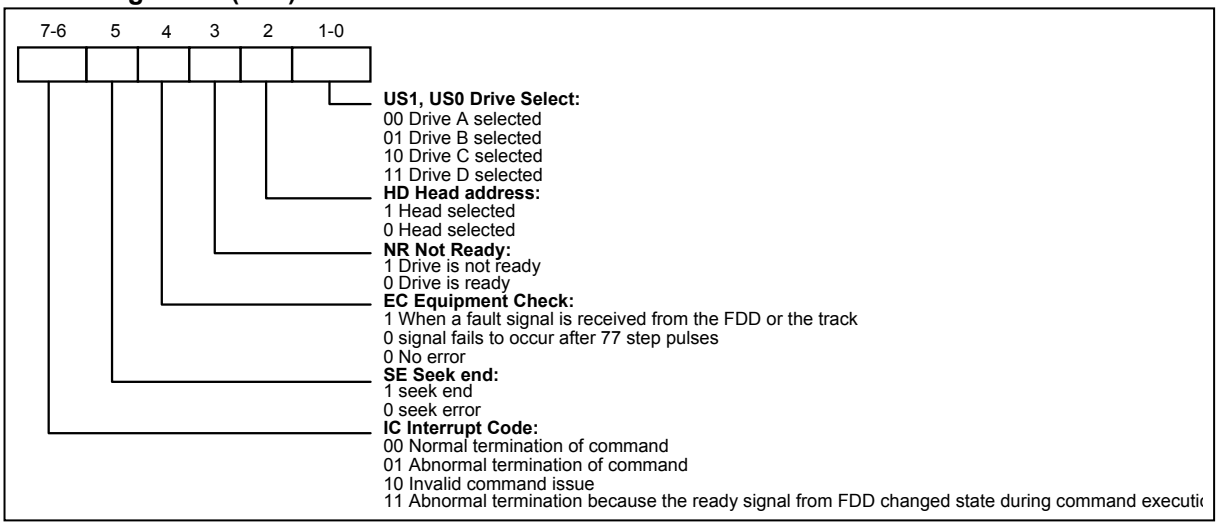
11 1 MB/S (MFM), Illegal (FM), $\overline{RWC}$ = 1.

The 2MB/S data rate for Tape drive is only supported by setting 01 to DRATE1 and DRATE0 bits, as well as setting 10 to DRTA1 and DRTA0 bits which are two of the Configuration CR2D. Please refer to the function of CR2D and the data rate table for individual data rates setting.

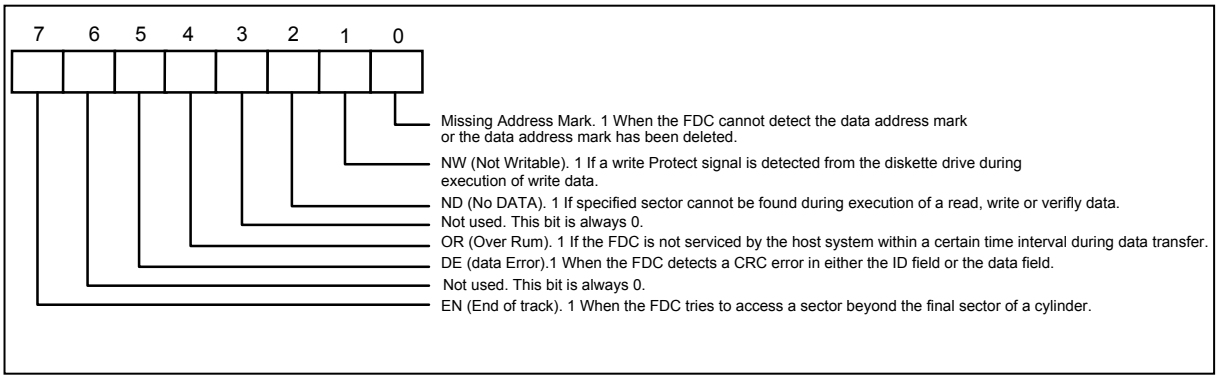
### 5.2.7 FIFO Register (R/W base address + 5)

The Data Register consists of four status registers in a stack with only one register presented to the data bus at a time. This register stores data, commands, and parameters and provides diskette-drive status information. Data bytes are passed through the data register to program or obtain results after a command. In the W83877TF/TG, this register defaults to FIFO disabled mode after reset. The FIFO can change its value and enable its operation through the CONFIGURE command.

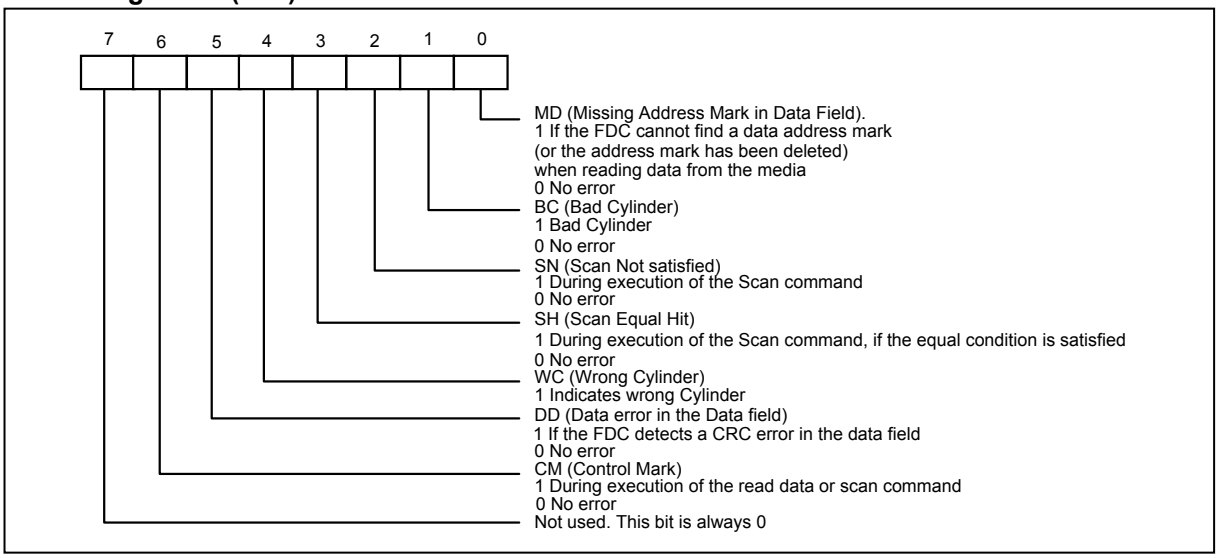
**Status Register 0 (ST0)**



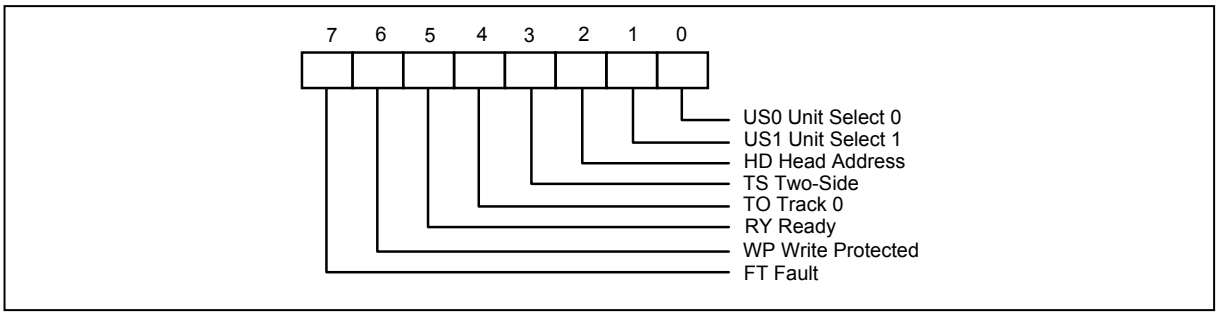

**Status Register 1 (ST1)**



**Status Register 2 (ST2)**

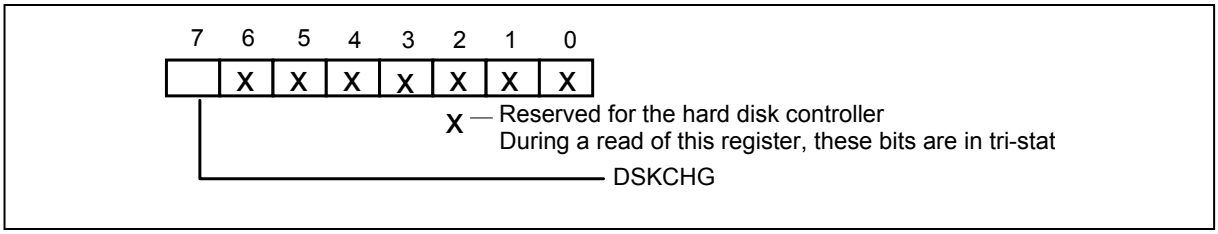



**Status Register 3 (ST3)**

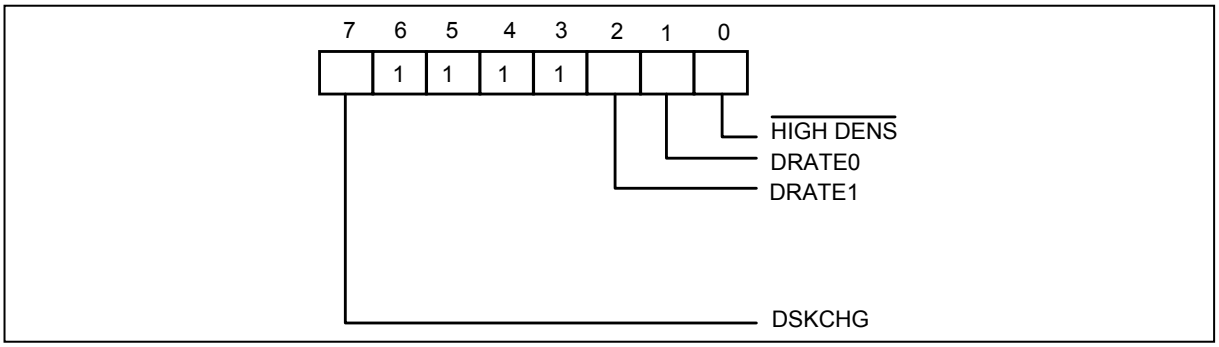



### 5.2.8 Digital Input Register (DI Register) (Read base address + 7)

The Digital Input Register is an 8-bit read-only register used for diagnostic purposes. In a PC/XT or AT only Bit 7 is checked by the BIOS. When the register is read, Bit 7 shows the complement of $\overline{\text{DSKCHG}}$, while other bits of the data bus remain in tri-state. Bit definitions are as follows:



In the PS/2 mode, the bit definitions are as follows:




DSKCHG (Bit 7):

This bit indicates the complement of the $\overline{\text{DSKCHG}}$ input.

Bit 6-3: These bits are always a logic 1 during a read.

DRATE1 DRATE0 (Bit 2, 1):

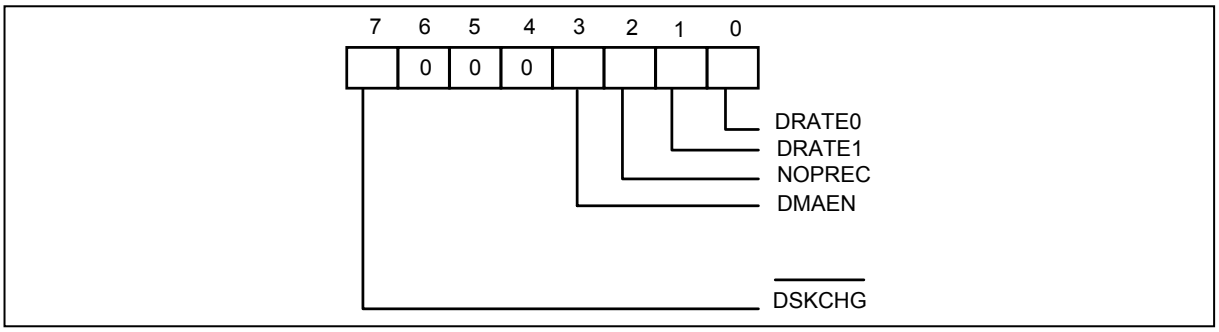
These two bits select the data rate of the FDC. Refer to the DR register bits 1 and 0 for the settings corresponding to the individual data rates.

$\overline{\text{HIGH DENS}}$ (Bit 0):

0 500 KB/S or 1 MB/S data rate (high density FDD)

1 250 KB/S or 300 KB/S data rate

In the PS/2 Model 30 mode, the bit definitions are as follows:




DSKCHG (Bit 7):

This bit indicates the status of $\overline{\text{DSKCHG}}$ input.

Bit 6-4: These bits are always a logic 1 during a read.

DMAEN (Bit 3):

This bit indicates the value of DO REGISTER bit 3.

NOPREC (Bit 2):

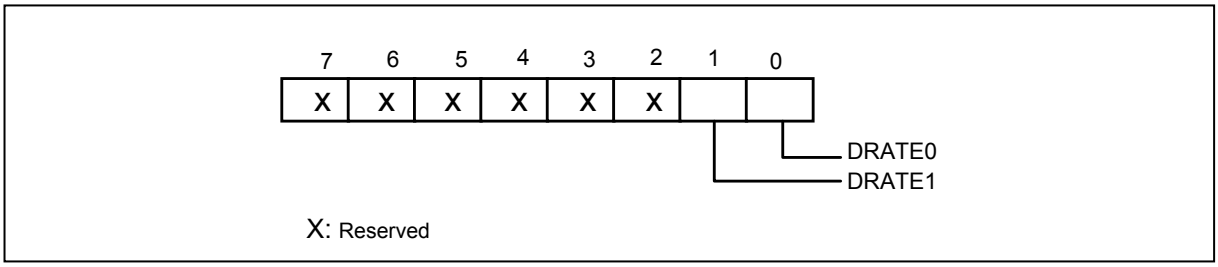
This bit indicates the value of CC REGISTER NOPREC bit.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

### 5.2.9 Configuration Control Register (CC Register) (Write base address + 7)

This register is used to control the data rate. In the PC/AT and PS/2 mode, the bit definitions are as follows:

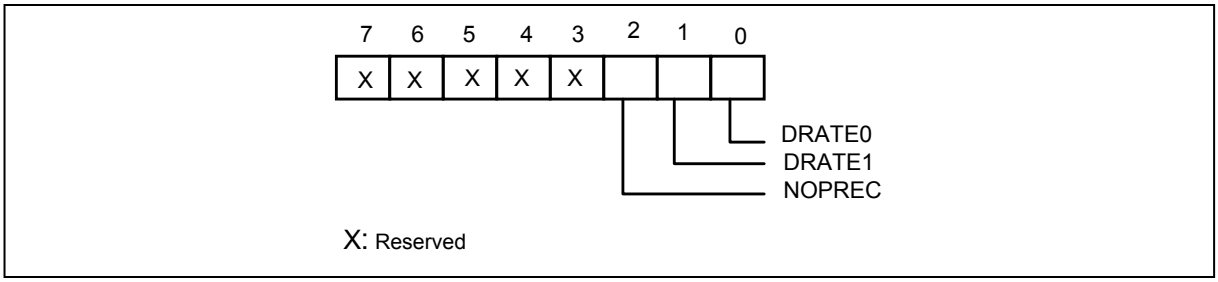



Bit 7-2: Reserved. These bits should be set to 0.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

In the PS/2 Model 30 mode, the bit definitions are as follows:




Bit 7-3: Reserved. These bits should be set to 0.

NOPREC (Bit 2):

This bit indicates no precompensation. It has no function and can be set by software.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

# 6. UART PORT

## 6.1 Universal Asynchronous Receiver/Transmitter (UART A, UART B)

The UARTs are used to convert parallel data into serial format on the transmit side and convert serial data to parallel format on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The UARTs are capable of handling divisors of 1 to 65535 and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. The UARTs also support the MIDI data rate. Furthermore, the UARTs also include complete modem control capability and a processor interrupt system that may be software trailed to the computing time required to handle the communication link. The UARTs have a FIFO mode to reduce the number of interrupts presented to the CPU. In each UART, there are 16-byte FIFOs for both receive and transmit mode.

## 6.2 Register Address

TABLE 6-1 UART Register Bit Map

| BIT NUMBER | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **REGISTER ADDRESS BASE** | | | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| 8 BDLAB = 0 | Receiver Buffer Register (Read Only) | RBR | RX Data Bit 0 | RX Data Bit 1 | RX Data Bit 2 | RX Data Bit 3 | RX Data Bit 4 | RX Data Bit 5 | RX Data Bit 6 | RX Data Bit 7 |
| 8 BDLAB = 0 | Transmitter Buffer Register (Write Only) | TBR | TX Data Bit 0 | TX Data Bit 1 | TX Data Bit 2 | TX Data Bit 3 | TX Data Bit 4 | TX Data Bit 5 | TX Data Bit 6 | TX Data Bit 7 |
| 9 BDLAB = 0 | Interrupt Control Register | ICR | RBR Data Ready Interrupt Enable (ERDRI) | TBR Empty Interrupt Enable (ETBREI) | USR Interrupt Enable (EUSRI) | HSR Interrupt Enable (EHSRI) | 0 | 0 | 0 | 0 |
| A | Interrupt Status Register (Read Only) | ISR | "0" if Interrupt Pending | Interrupt Status Bit (0) | Interrupt Status Bit (1) | Interrupt Status Bit (2)** | 0 | 0 | FIFOs Enabled ** | FIFOs Enabled ** |
| A | UART FIFO Control Register (Write Only) | UFR | FIFO Enable | RCVR FIFO Reset | XMIT FIFO Reset | DMA Mode Select | Reserved | Reversed | RX Interrupt Active Level (LSB) | RX Interrupt Active Level (MSB) |
| B | UART Control Register | UCR | Data Length Select Bit 0 (DLS0) | Data Length Select Bit 1 (DLS1) | Multiple Stop Bits Enable (MSBE) | Parity Bit Enable (PBE) | Even Parity Enable (EPE) | Parity Bit Fixed Enable PBFE) | Set Silence Enable (SSE) | Baud rate Divisor Latch Access Bit (BDLAB) |
| C | Handshake Control Register | HCR | Data Terminal Ready (DTR) | Request to Send (RTS) | Loopback RI Input | IRQ Enable | Internal Loopback Enable | 0 | 0 | 0 |

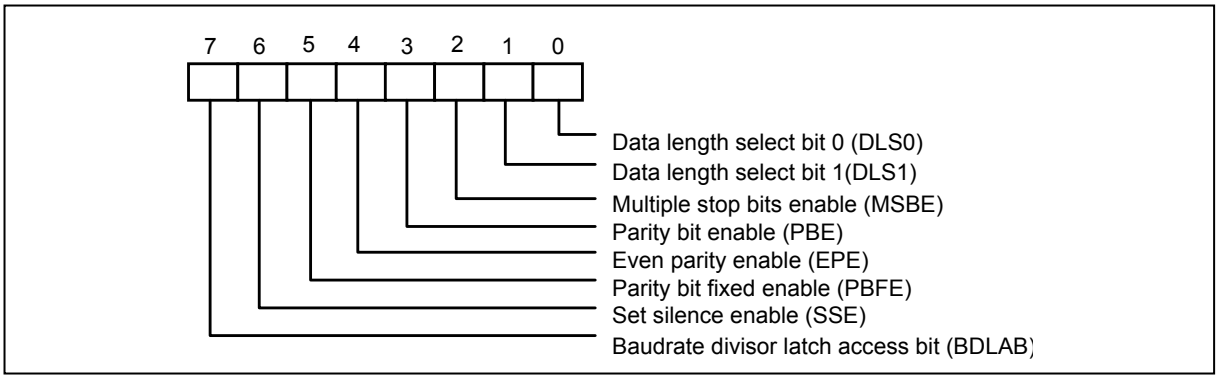
Register Address, continued.

| BIT NUMBER | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **REGISTER ADDRESS BASE** | | | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| D | UART Status Register | USR | RBR Data Ready (RDR) | Overrun Error (OER) | Parity Bit Error (PBER) | No Stop Bit Error (NSER) | Silent Byte Detected (SBD) | TBR Empty (TBRE) | TSR Empty (TSRE) | RX FIFO Error Indication (RFEI) ** |
| E | Handshake Status Register | HSR | CTS Toggling (TCTS) | DSR Toggling (TDSR) | RI Falling Edge (FERI) | DCD Toggling (TDCD) | Clear to Send (CTS) | Data Set Ready (DSR) | Ring Indicator (RI) | Data Carrier Detect (DCD) |
| F | User Defined Register | UDR | Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 |
| 8 BDLAB = 1 | Baudrate Divisor Latch Low | BLL | Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 |
| 9 BDLAB = 1 | Baudrate Divisor Latch High | BHL | Bit 8 | Bit 9 | Bit 10 | Bit 11 | Bit 12 | Bit 13 | Bit 14 | Bit 15 |

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.
**: These bits are always 0 in 16450 mode.

### 6.2.1 UART Control Register (UCR) (Read/Write)

The UART Control Register controls and defines the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.




Bit 7: BDLAB. When this bit is set to a logical 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud rate generator during a read or write operation. When this bit is reset, the Receiver Buffer Register, the Transmitter Buffer Register, or the Interrupt Control Register can be accessed.

Bit 6: SSE. A logical 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only SOUT is affected by this bit; the transmitter is not affected.

Bit 5: PBFE. When PBE and PBFE of UCR are both set to a logical 1,

(1) if EPE is a logical 1, the parity bit is fixed as a logical 0 to transmit and check.

(2) if EPE is a logical 0, the parity bit is fixed as a logical 1 to transmit and check.

Bit 4: EPE. This bit describes the number of logic 1's in the data word bits and parity bit only when bit 3 is programmed. When this bit is set, an even number of logic 1's are sent or checked. When the bit is reset, an odd number of logic 1's are sent or checked.

Bit 3: PBE. When this bit is set, the position between the last data bit and the stop bit of the SOUT will be stuffed with the parity bit at the transmitter. For the receiver, the parity bit in the same position as the transmitter will be detected.

Bit 2: MSBE. This bit defines the number of stop bits in each serial character that is transmitted or received.

(1) If MSBE is set to a logical 0, one stop bit is sent and checked.

(2) If MSBE is set to a logical 1, and data length is 5 bits, one and a half stop bits are sent and checked.

(3) If MSBE is set to a logical 1, and data length is 6, 7, or 8 bits, two stop bits are sent and checked.

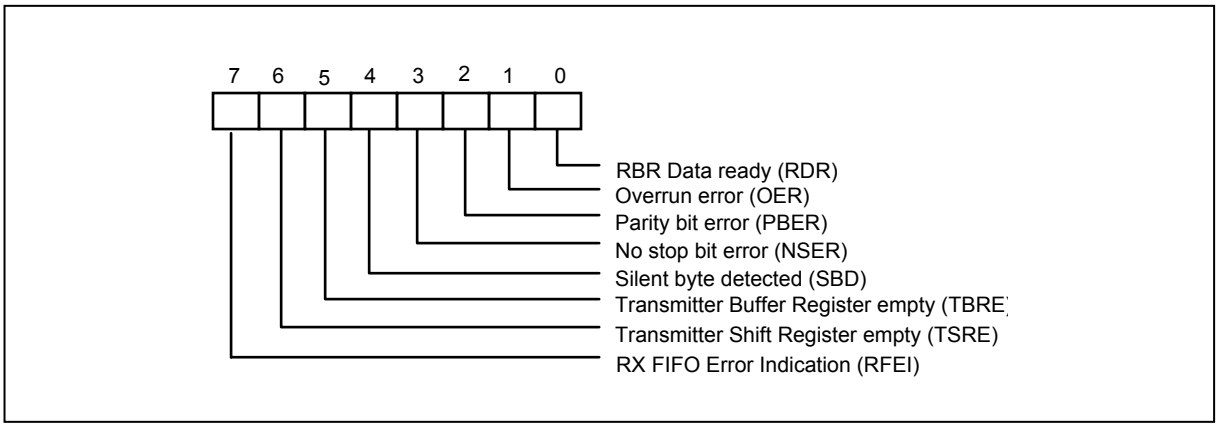
Bits 0 and 1: DLS0, DLS1. These two bits define the number of data bits that are sent or checked in each serial character.

TABLE 6-2 WORD LENGTH DEFINITION

| DLS1 | DLS0 | DATA LENGTH |
|---|---|---|
| 0 | 0 | 5 bits |
| 0 | 1 | 6 bits |
| 1 | 0 | 7 bits |
| 1 | 1 | 8 bits |

### 6.2.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of the data transfer during communication.




Bit 7: RFEI. In 16450 mode, this bit is always set to a logic 0. In 16550 mode, this bit is set to a logic 1 when there is at least one parity bit error, no stop bit error or silent byte detected in the FIFO. In 16550 mode, this bit is cleared by reading from the USR if there are no remaining errors left in the FIFO.

Bit 6: TSRE. In 16450 mode, when TBR and TSR are both empty, this bit will be set to a logical 1. In 16550 mode, if the transmit FIFO and TSR are both empty, it will be set to a logical 1. Other than these two cases, this bit will be reset to a logical 0.

Bit 5: TBRE. In 16450 mode, when a data character is transferred from TBR to TSR, this bit will be set to a logical 1. If ETREI of ICR is a logical 1, an interrupt will be generated to notify the CPU to write the next data. In 16550 mode, this bit will be set to a logical 1 when the transmit FIFO is empty. It will be reset to a logical 0 when the CPU writes data into TBR or FIFO.

Bit 4: SBD. This bit is set to a logical 1 to indicate that received data are kept in silent state for a full word time, including start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 3: NSER. This bit is set to a logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

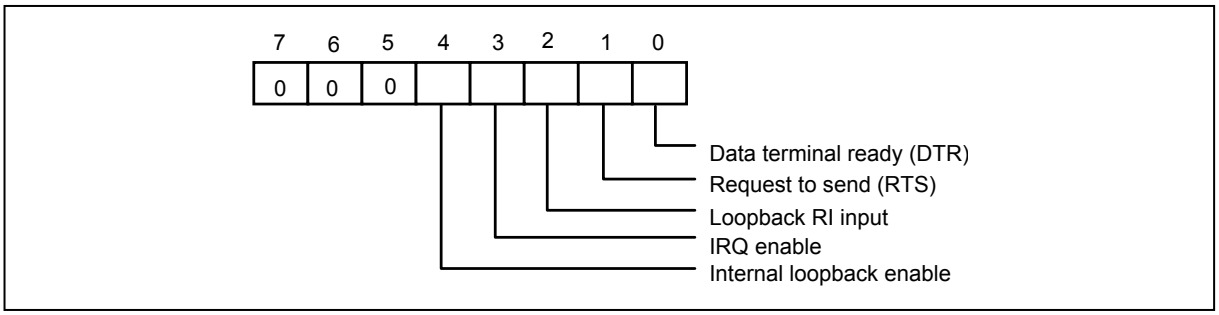
Bit 2: PBER. This bit is set to a logical 1 to indicate that the parity bit of received data is wrong. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 1: OER. This bit is set to a logical 1 to indicate received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition instead of FIFO full. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 0: RDR. This bit is set to a logical 1 to indicate received data are ready to be read by the CPU in the RBR or FIFO. After no data are left in the RBR or FIFO, the bit will be reset to a logical 0.

### 6.2.3 Handshake Control Register (HCR) (Read/Write)

This register controls the pins of the UART used for handshaking peripherals such as modem, and controls the diagnostic mode of the UART.




Bit 4: When this bit is set to a logical 1, the UART enters diagnostic mode by an internal loopback, as follows:

(1) SOUT is forced to a logical 1, and SIN is isolated from the communication link instead of the TSR.

(2) Modem output pins are set to their inactive state.

(3) Modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) → $\overline{DSR}$, RTS ( bit 1 of HCR) → $\overline{CTS}$, Loopback RI input ( bit 2 of HCR) → $\overline{RI}$ and IRQ enable ( bit 3 of HCR) → $\overline{DCD}$.

Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.

Bit 3: The UART interrupt output is enabled by setting this bit to a logic 1. In the diagnostic mode this bit is internally connected to the modem control input $\overline{DCD}$.

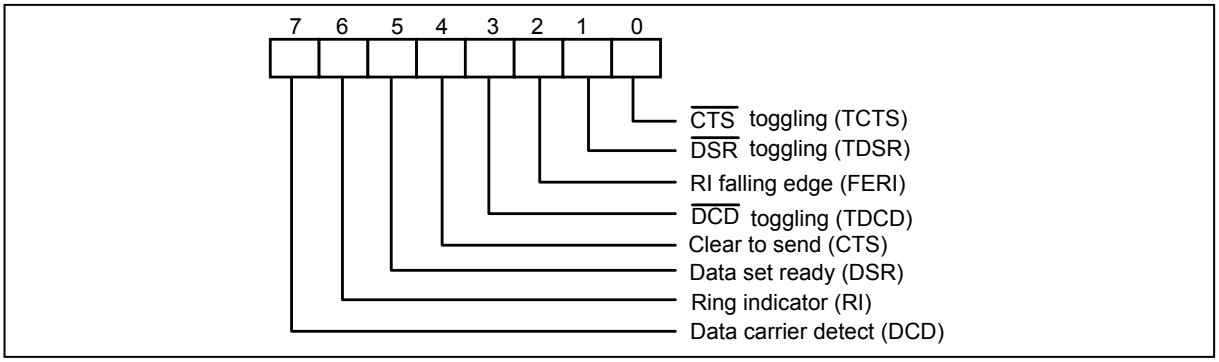
Bit 2: This bit is used only in the diagnostic mode. In the diagnostic mode this bit is internally connected to the modem control input $\overline{RI}$.

Bit 1: This bit controls the $\overline{RTS}$ output. The value of this bit is inverted and output to $\overline{RTS}$.

Bit 0: This bit controls the $\overline{DTR}$ output. The value of this bit is inverted and output to $\overline{DTR}$.

### 6.2.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins for handshake peripherals such as a modem and records changes on these pins.




Bit 7: This bit is the opposite of the $\overline{DCD}$ input. This bit is equivalent to bit 3 of HCR in loopback mode.

Bit 6: This bit is the opposite of the $\overline{RI}$ input. This bit is equivalent to bit 2 of HCR in loopback mode.

Bit 5: This bit is the opposite of the $\overline{DSR}$ input. This bit is equivalent to bit 0 of HCR in loopback mode.

Bit 4: This bit is the opposite of the $\overline{CTS}$ input. This bit is equivalent to bit 1 of HCR in loopback mode.

Bit 3: TDCD. This bit indicates that the $\overline{DCD}$ pin has changed state after HSR was read by the CPU.

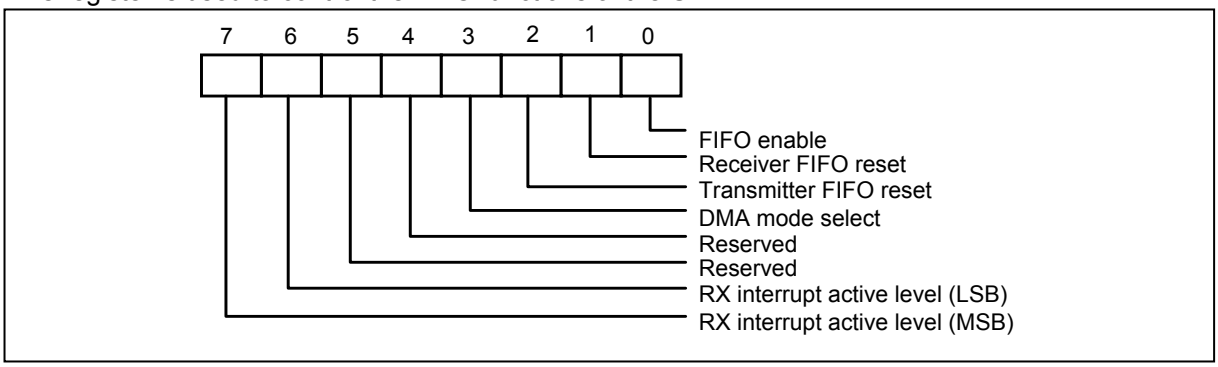
Bit 2: FERI. This bit indicates that the $\overline{RI}$ pin has changed from low to high state after HSR was read by the CPU.

Bit 1: TDSR. This bit indicates that the $\overline{DSR}$ pin has changed state after HSR was read by the CPU.

Bit 0: TCTS. This bit indicates that the $\overline{CTS}$ pin has changed state after HSR was read by the CPU.

### 6.2.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.




Bit 6, 7: These two bits are used to set the active level for the receiver FIFO interrupt. For example, if the interrupt active level is set as 4 bytes, once there are more than 4 data characters in the receiver FIFO, the interrupt will be activated to notify the CPU to read the data from the FIFO.

TABLE 6-3 FIFO TRIGGER LEVEL

| BIT 7 | BIT 6 | RX FIFO INTERRUPT ACTIVE LEVEL (BYTES) |
|---|---|---|
| 0 | 0 | 01 |
| 0 | 1 | 04 |
| 1 | 0 | 08 |
| 1 | 1 | 14 |

Bit 4, 5: Reserved

Bit 3: When this bit is programmed to logic 1, the DMA mode will change from mode 0 to mode 1 if UFR bit 0 = 1.

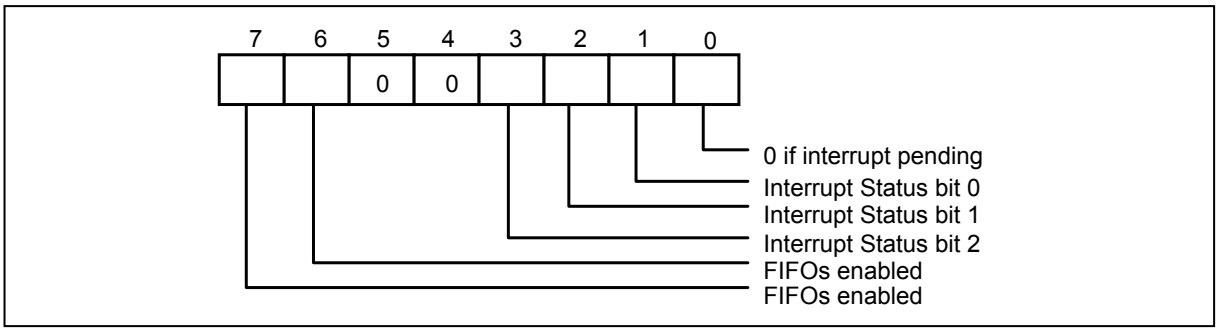
Bit 2: Setting this bit to a logical 1 resets the TX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 1: Setting this bit to a logical 1 resets the RX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 0: This bit enables the 16550 (FIFO) mode of the UART. This bit should be set to a logical 1 before other bits of UFR are programmed.

### 6.2.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status, which is encoded by different interrupt sources into 3 bits.




Bit 7, 6: These two bits are set to a logical 1 when UFR bit 0 = 1.

Bit 5, 4: These two bits are always logic 0.

Bit 3: In 16450 mode, this bit is 0. In 16550 mode, both bit 3 and 2 are set to a logical 1 when a time-out interrupt is pending.

Bit 2, 1: These two bits identify the priority level of the pending interrupt, as shown in the table below.

Bit 0: This bit is a logical 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit will be set to a logical 0.

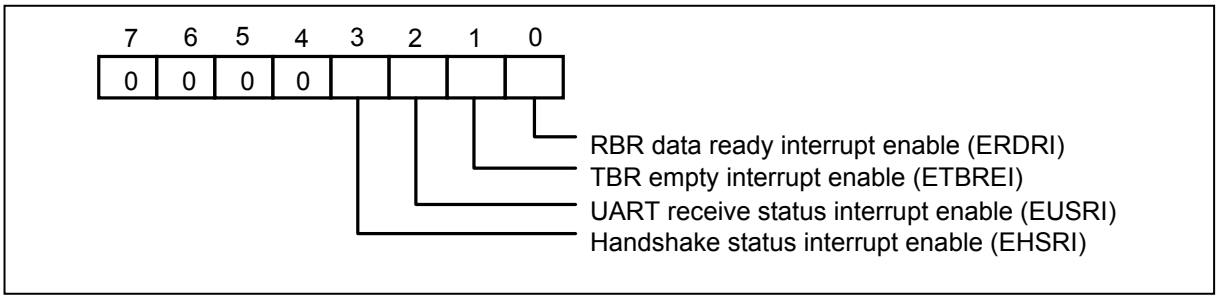
TABLE 6-4 INTERRUPT CONTROL FUNCTION

| ISR | | | | INTERRUPT SET AND FUNCTION | | | |
|---|---|---|---|---|---|---|---|
| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Interrupt priority | Interrupt Type | Interrupt Source | Clear Interrupt |
| 0 | 0 | 0 | 1 | - | - | No Interrupt pending | - |
| 0 | 1 | 1 | 0 | First | UART Receive Status | 1. OER = 1 2. PBER =1<br>3. NSER = 1 4. SBD = 1 | Read USR |
| 0 | 1 | 0 | 0 | Second | RBR Data Ready | 1. RBR data ready<br>2. FIFO interrupt active level reached | 1. Read RBR<br>2. Read RBR until FIFO data under active level |
| 1 | 1 | 0 | 0 | Second | FIFO Data Timeout | Data present in RX FIFO for 4 characters period of time since last access of RX FIFO. | Read RBR |
| 0 | 0 | 1 | 0 | Third | TBR Empty | TBR empty | 1. Write data into TBR<br>2. Read ISR (if priority is third) |
| 0 | 0 | 0 | 0 | Fourth | Handshake status | 1. TCTS = 1 2. TDSR = 1<br>3. FERI = 1 4. TDCD = 1 | Read HSR |

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

### 6.2.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register allows the five types of controller interrupts to activate the interrupt output signal separately. The interrupt system can be totally disabled by resetting bits 0 through 3 of the Interrupt Control Register (ICR). A selected interrupt can be enabled by setting the appropriate bits of this register to a logical 1.




Bit 7-4: These four bits are always logic 0.

Bit 3: EHSRI. Setting this bit to a logical 1 enables the handshake status register interrupt.

Bit 2: EUSRI. Setting this bit to a logical 1 enables the UART status register interrupt.

Bit 1: ETBREI. Setting this bit to a logical 1 enables the TBR empty interrupt.

Bit 0: ERDRI. Setting this bit to a logical 1 enables the RBR data ready interrupt.

### 6.2.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divides it by a divisor from 1 to $2^{16}$-1. The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (refer to CR0C bit7 and CR0C bit6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. In high-speed mode, the data transmission rate can be as high as 1.5M bps.

### 6.2.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

TABLE 6-5 BAUD RATE TABLE

| BAUD RATE USING 24 MHZ TO GENERATE 1.8461 MHZ | | |
|---|---|---|
| **DESIRED BAUD RATE** | **DECIMAL DIVISOR USED TO GENERATE 16X CLOCK** | **PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL** |
| 50 | 2304 | ** |
| 75 | 1536 | ** |
| 110 | 1047 | 0.18% |
| 134.5 | 857 | 0.099% |
| 150 | 768 | ** |
| 300 | 384 | ** |
| 600 | 192 | ** |
| 1200 | 96 | ** |
| 1800 | 64 | ** |
| 2000 | 58 | 0.53% |
| 2400 | 48 | ** |
| 3600 | 32 | ** |
| 4800 | 24 | ** |
| 7200 | 16 | ** |
| 9600 | 12 | ** |
| 19200 | 6 | ** |
| 38400 | 3 | ** |
| 57600 | 2 | ** |
| 115200 | 1 | ** |
| 230400 | 4 Note 1 | ** |
| 460800 | 2 Note 1 | ** |
| 921600 | 1 Note 1 | ** |
| 1.5M | 1 Note 2 | 0% |

**Note 1:** Only use in high speed mode, when FASTA/FASTB bits are set (refer to CR19 bit1 and CR19 bit0).

**Note 2:** Only use in high speed mode, when TURA/TURB bits are set (refer to CR0C bit7 and bit6).

** The percentage error for all baud rates, except where indicated otherwise, is 0.16%

# 7. PARALLEL PORT

## 7.1 Printer Interface Logic

The parallel port of the W83877TF/TG makes possible the attachment of various devices that accept eight bits of parallel data at standard TTL level. W83877TF/TG supports an IBM XT/AT compatible parallel port (SPP), bi-directional parallel port (BPP), Enhanced Parallel Port (EPP), Extended Capabilities Parallel Port (ECP), Extension FDD mode (EXTFDD), and Extension 2FDD mode (EXT2FDD) on the parallel port. Refer to the configuration registers for more information on disabling, power-down, and on selecting the mode of operation.

Table 7-1 shows the pin definitions for different modes of the parallel port.

**TABLE 7-1-A Parallel Port Connector and Pin Definition for SPP/EPP/ECP Modes**

| HOST CONNECTOR | PIN NUMBER OF W83877TF | PIN ATTRIBUTE | SPP | EPP | ECP |
|---|---|---|---|---|---|
| 1 | 19 | O | nSTB | nWrite | nSTB, HostClk |
| 2-9 | 9-14,16-17 | I/O | PD<0:7> | PD<0:7> | PD<0:7> |
| 10 | 26 | I | nACK | Intr | nACK, PeriphClk |
| 11 | 24 | I | BUSY | nWait | BUSY, PeriphAck[2] |
| 12 | 27 | I | PE | PE | PEerror, nAckReverse[2] |
| 13 | 28 | I | SLCT | Select | SLCT, Xflag |
| 14 | 20 | O | nAFD | nDStrb | nAFD, HostAck[2] |
| 15 | 29 | I | nERR | nError | nFault[1], nPeriphRequest[2] |
| 16 | 21 | O | nINIT | nInit | nINIT[1], nReverseRqst[2] |
| 17 | 22 | O | nSLIN | nAStrb | nSLIN[1] , ECPMode[2] |

**Notes:**

n<name > : Active Low

1. Compatible Mode

2. High Speed Mode

3. For more information, refer to the IEEE 1284 standard.

**TABLE 7-1-B Parallel Port Connector and Pin Definition for EXTFDD and EXT2FDD Modes**

| HOST CONNECTOR | PIN NUMBER OF W83877TF | PIN ATTRIBUTE | SPP | PIN ATTRIBUTE | EXT2FDD | PIN ATTRIBUTE | EXTFDD |
|---|---|---|---|---|---|---|---|
| 1 | 19 | O | nSTB | --- | --- | --- | --- |
| 2 | 9 | I/O | PD0 | I | $\overline{\text{INDEX2}}$ | I | $\overline{\text{INDEX2}}$ |
| 3 | 10 | I/O | PD1 | I | $\overline{\text{TRAK02}}$ | I | |
| 4 | 11 | I/O | PD2 | I | $\overline{\text{WP2}}$ | I | |
| 5 | 12 | I/O | PD3 | I | $\overline{\text{RDATA2}}$ | I | $\overline{\text{RDATA2}}$ |
| 6 | 13 | I/O | PD4 | I | $\overline{\text{DSKCHG2}}$ | I | $\overline{\text{DSKCHG}}$ |
| 7 | 14 | I/O | PD5 | --- | --- | --- | --- |
| 8 | 15 | I/O | PD6 | OD | $\overline{\text{MOA2}}$ | --- | --- |
| 9 | 16 | I/O | PD7 | OD | $\overline{\text{DSA2}}$ | --- | --- |
| 10 | 26 | I | nACK | OD | $\overline{\text{DSB2}}$ | OD | |
| 11 | 24 | I | BUSY | OD | $\overline{\text{MOB2}}$ | OD | |
| 12 | 27 | I | PE | OD | $\overline{\text{WD2}}$ | OD | $\overline{\text{WD2}}$ |
| 13 | 28 | I | SLCT | OD | $\overline{\text{WE2}}$ | OD | $\overline{\text{WE2}}$ |
| 14 | 20 | O | nAFD | OD | $\overline{\text{RWC2}}$ | OD | $\overline{\text{RWC2}}$ |
| 15 | 29 | I | nERR | OD | $\overline{\text{NERR2}}$ | OD | |
| 16 | 21 | O | nINIT | OD | $\overline{\text{DIR2}}$ | OD | $\overline{\text{DIR2}}$ |
| 17 | 22 | O | nSLIN | OD | $\overline{\text{STEP2}}$ | OD | |

## 7.2 Enhanced Parallel Port (EPP)

**TABLE 7-2 PRINTER MODE AND EPP REGISTER ADDRESS**

| A2 | A1 | A0 | REGISTER | NOTE |
|---|---|---|---|---|
| 0 | 0 | 0 | Data port (R/W) | 1 |
| 0 | 0 | 1 | Printer status buffer (Read) | 1 |
| 0 | 1 | 0 | Printer control latch (Write) | 1 |
| 0 | 1 | 0 | Printer control swapper (Read) | 1 |
| 0 | 1 | 1 | EPP address port (R/W) | 2 |
| 1 | 0 | 0 | EPP data port 0 (R/W) | 2 |
| 1 | 0 | 1 | EPP data port 1 (R/W) | 2 |
| 1 | 1 | 0 | EPP data port 2 (R/W) | 2 |
| 1 | 1 | 1 | EPP data port 2 (R/W) | 2 |

**Notes:**

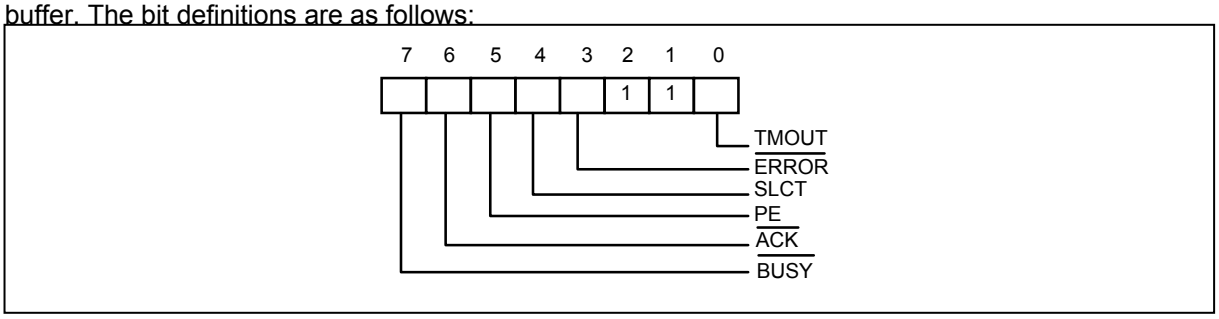
1. These registers are available in all modes.
2. These registers are available only in EPP mode.

### 7.2.1 Data Swapper

The system microprocessor can read the contents of the printer's data latch by reading the data swapper.

### 7.2.2 Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the printer status buffer. The bit definitions are as follows:




Bit 7: This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.

Bit 6: This bit represents the current state of the printer's $\overline{ACK}$ signal. A 0 means the printer has received a character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before $\overline{BUSY}$ stops.

Bit 5: A 1 means the printer has detected the end of paper.

Bit 4: A 1 means the printer is selected.

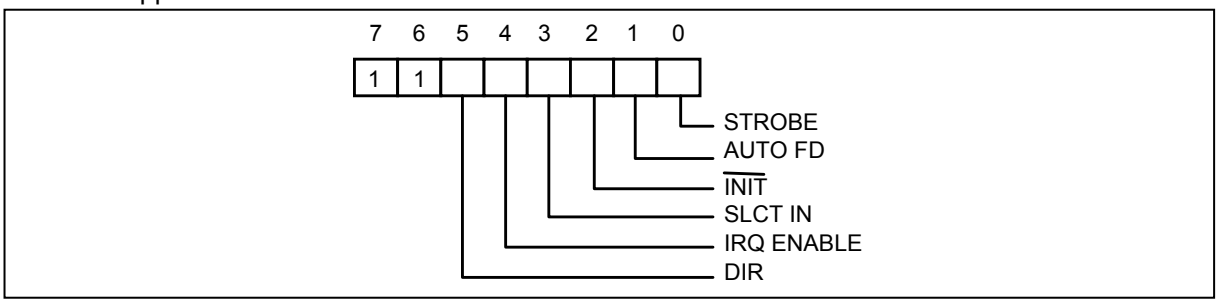
Bit 3: A 0 means the printer has encountered an error condition.

Bit 1, 2: These two bits are not implemented and are logic one during a read of the status register.

Bit 0: This bit is valid in EPP mode only. It indicates that a 10 μS time-out has occurred on the EPP bus. A logic 0 means that no time-out error has occurred; a logic 1 means that a time-out error has been detected. Writing a logic 1 to this bit will clear the time-out status bit; writing a logic 0 has no effect.

### 7.2.3 Printer Control Latch and Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the printer control swapper. Bit definitions are as follows:




Bit 7, 6: These two bits are a logic one during a read. They can be written.

Bit 5: Direction control bit

When this bit is a logic 1, the parallel port is in input mode (read); when it is a logic 0, the parallel port is in output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.

Bit 4: A 1 in this position allows an interrupt to occur when $\overline{\text{ACK}}$ changes from low to high.

Bit 3: A 1 in this bit position selects the printer.

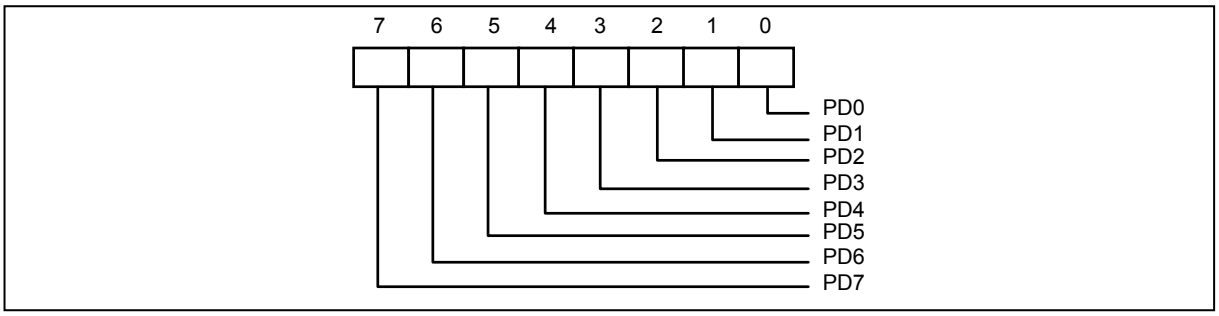
Bit 2: A 0 starts the printer (50 microsecond pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum high active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

### 7.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

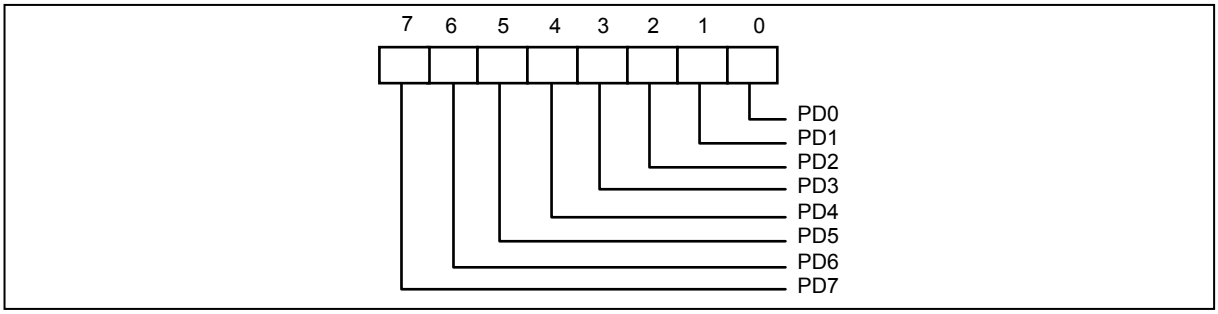


The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of $\overline{IOW}$ causes an EPP address write cycle to be performed, and the trailing edge of $\overline{IOW}$ latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of $\overline{IOR}$ causes an EPP address read cycle to be performed and the data to be output to the host CPU.

### 7.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. Bit definitions of each data port are as follows:




When accesses are made to any EPP data port, the contents of DB0-DB7 are buffered (non-inverting) and output to the ports PD0-PD7 during a write operation. The leading edge of $\overline{IOW}$ causes an EPP data write cycle to be performed, and the trailing edge of $\overline{IOW}$ latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of $\overline{IOR}$ causes an EPP read cycle to be performed and the data to be output to the host CPU.

### 7.2.6 Bit Map of Parallel Port and EPP Registers

| REGISTER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Data Port (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Status Buffer (Read) | $\overline{BUSY}$ | $\overline{ACK}$ | PE | SLCT | $\overline{ERROR}$ | 1 | 1 | TMOUT |
| Control Swapper (Read) | 1 | 1 | 1 | IRQEN | SLIN | $\overline{INIT}$ | $\overline{AUTOFD}$ | $\overline{STROBE}$ |
| Control Latch (Write) | 1 | 1 | DIR | IRQ | SLIN | $\overline{INIT}$ | $\overline{AUTOFD}$ | $\overline{STROBE}$ |
| EPP Address Port (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 0 (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 1 (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 2 (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 3 (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |

### 7.2.7 EPP Pin Descriptions

| EPP NAME | TYPE | EPP DESCRIPTION |
|---|---|---|
| nWrite | O | Denotes an address or data read or write operation. |
| PD<0:7> | I/O | Bi-directional EPP address and data bus. |
| Intr | I | Used by peripheral device to interrupt the host. |
| nWait | I | Inactive to acknowledge that data transfer is completed. Active to indicate that the device is ready for the next transfer. |
| PE | I | Paper end; same as SPP mode. |
| Select | I | Printer selected status; same as SPP mode. |
| nDStrb | O | This signal is active low. It denotes a data read or write operation. |
| nError | I | Error; same as SPP mode. |
| nInits | O | This signal is active low. When it is active, the EPP device is reset to its initial operating mode. |
| nAStrb | O | This signal is active low. It denotes an address read or write operation. |

### 7.2.8 EPP Operation

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. The PDx bus is in the standard or bi-directional mode when no EPP read, write, or address cycle is currently being executed. In this condition all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 μS have elapsed from the start of the EPP cycle to the time $\overline{WAIT}$ is de-asserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in Status bit 0.

EPP Operation

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed synchronously.

EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If the nWait is active low, when the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, the read/write cycle proceeds normally and will be completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle will not start. It must wait until nWait changes to active low, at which time it will start as described above.

EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it will not terminate until nWait changes from active low to inactive high.

## 7.3 Extended Capabilities Parallel (ECP) Port

This port is software and hardware compatible with existing parallel ports, so it may be used as a standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host to peripheral) and reverse (peripheral to host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port supports run-length-encoded (RLE) decompression (required) in the hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. The hardware support for compression is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

### 7.3.1 ECP Register and Mode Definitions

| NAME | ADDRESS | I/O | ECP MODES | FUNCTION |
|---|---|---|---|---|
| data | Base+000h | R/W | 000-001 | Data Register |
| ecpAFifo | Base+000h | R/W | 011 | ECP FIFO (Address) |
| dsr | Base+001h | R | All | Status Register |
| dcr | Base+002h | R/W | All | Control Register |
| cFifo | Base+400h | R/W | 010 | Parallel Port Data FIFO |
| ecpDFifo | Base+400h | R/W | 011 | ECP FIFO (DATA) |
| tFifo | Base+400h | R/W | 110 | Test FIFO |
| cnfgA | Base+400h | R | 111 | Configuration Register A |
| cnfgB | Base+401h | R/W | 111 | Configuration Register B |
| ecr | Base+402h | R/W | All | Extended Control Register |

**Note:** The base addresses are specified by CR23, which are determined by configuration register or hardware setting.

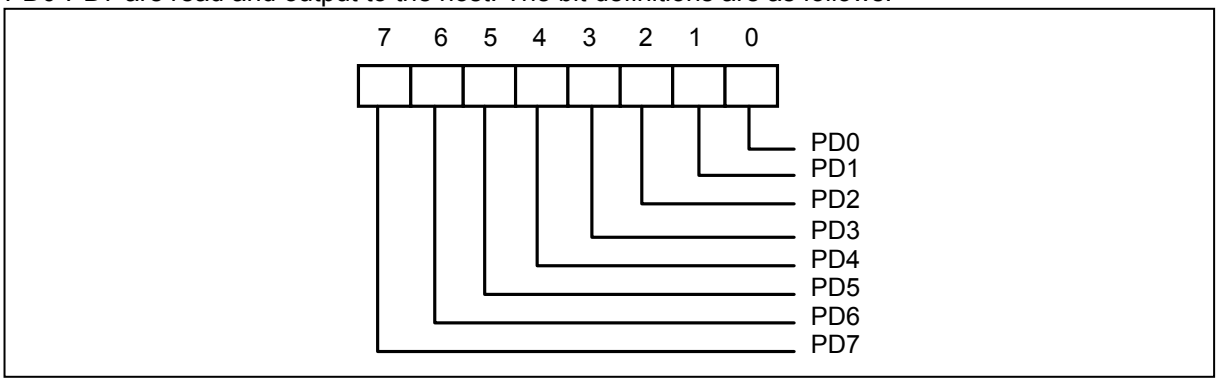
| MODE | DESCRIPTION |
|---|---|
| 000 | SPP mode |
| 001 | PS/2 Parallel Port mode |
| 010 | Parallel Port Data FIFO mode |
| 011 | ECP Parallel Port mode |
| 100 | EPP mode (If this option is enabled in the CR9 and CR0 to select ECP/EPP mode) |
| 101 | Reserved |
| 110 | Test mode |
| 111 | Configuration mode |

**Note:** The mode selection bits are bit 7-5 of the Extended Control Register.

### 7.3.2 Data and ecpAFifo Port

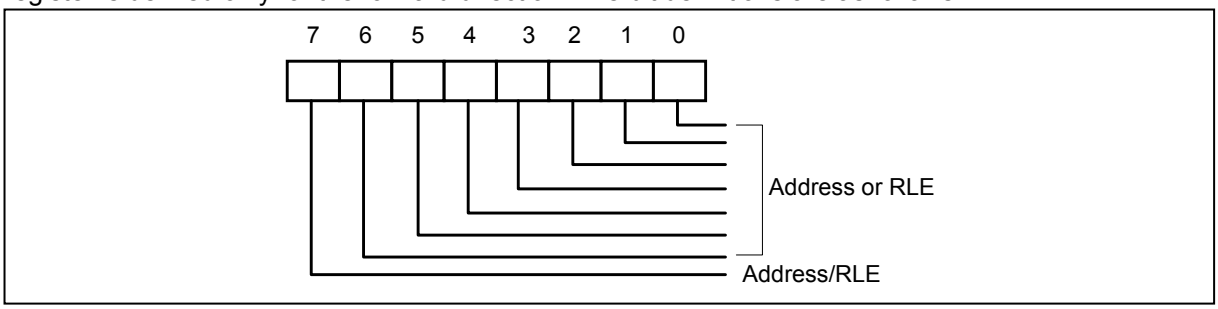
Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input. The contents of this register are output to the PD0-PD7 ports. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:



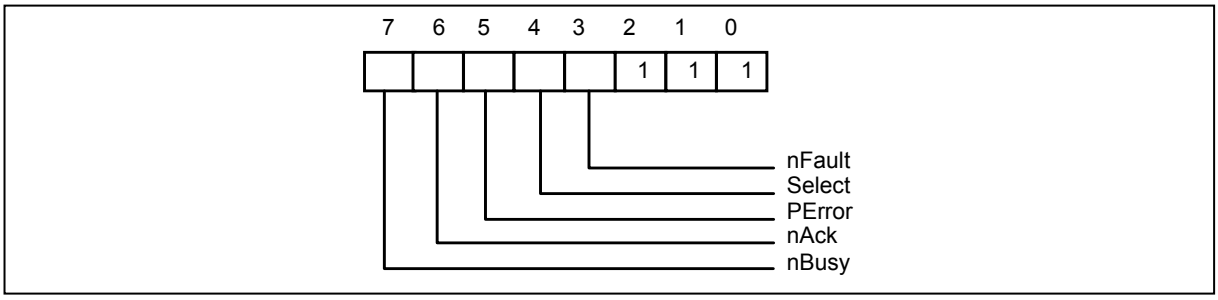

Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is defined only for the forward direction. The bit definitions are as follows:




### 7.3.3 Device Status Register (DSR)

These bits are at low level during a read of the Printer Status Register. The bits of this status register are defined as follows:




Bit 7: This bit reflects the complement of the Busy input.

Bit 6: This bit reflects the nAck input.

Bit 5: This bit reflects the PError input.

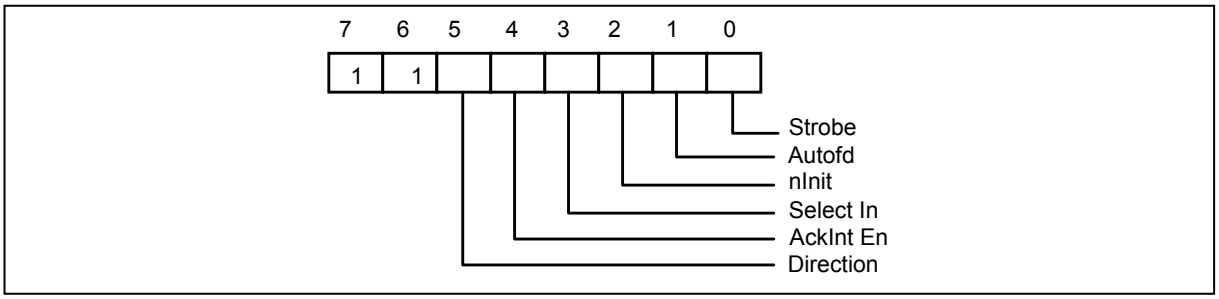
Bit 4: This bit reflects the Select input.

Bit 3: This bit reflects the nFault input.

Bit 2-0: These three bits are not implemented and are always logic one during a read.

### 7.3.4 Device Control Register (DCR)

The bit definitions are as follows:




Bit 6, 7: These two bits are logic one during a read and cannot be written.

Bit 5: This bit has no effect and the direction is always out if mode = 000 or mode = 010. Direction is valid in all other modes.

0 the parallel port is in output mode.

1 the parallel port is in input mode.

Bit 4: Interrupt request enable. When this bit is set to a high level, it may be used to enable interrupt requests from the parallel port to the CPU due to a low to high transition on the $\overline{ACK}$ input.

Bit 3: This bit is inverted and output to the $\overline{SLIN}$ output.

0 The printer is not selected.

1 The printer is selected.

Bit 2: This bit is output to the $\overline{INIT}$ output.

Bit 1: This bit is inverted and output to the $\overline{AFD}$ output.

Bit 0: This bit is inverted and output to the $\overline{STB}$ output.

### 7.3.5 cFifo (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. The standard parallel port protocol is used by a hardware handshake to the peripheral to transmit bytes written or DMAed from the system to this FIFO. Transfers to the FIFO are byte aligned.

### 7.3.6 ecpDFifo (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

When the direction bit is 1, data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

### 7.3.7 tFifo (Test FIFO Mode) Mode = 110

Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction.

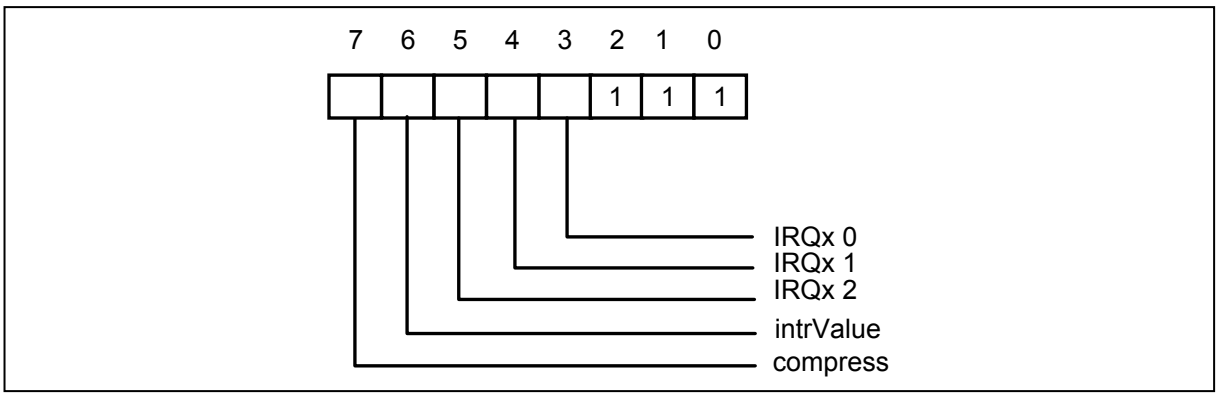
Data in the tFIFO will not be transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

### 7.3.8 cnfgA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates to the system that this is an 8-bit implementation.

### 7.3.9 cnfgB (Configuration Register B) Mode = 111

The bit definitions are as follows:




Bit 7: This bit is read-only. It is at low level during a read. This means that this chip does not support hardware RLE compression.

Bit 6: Returns the value on the ISA IRQ line to determine possible conflicts.

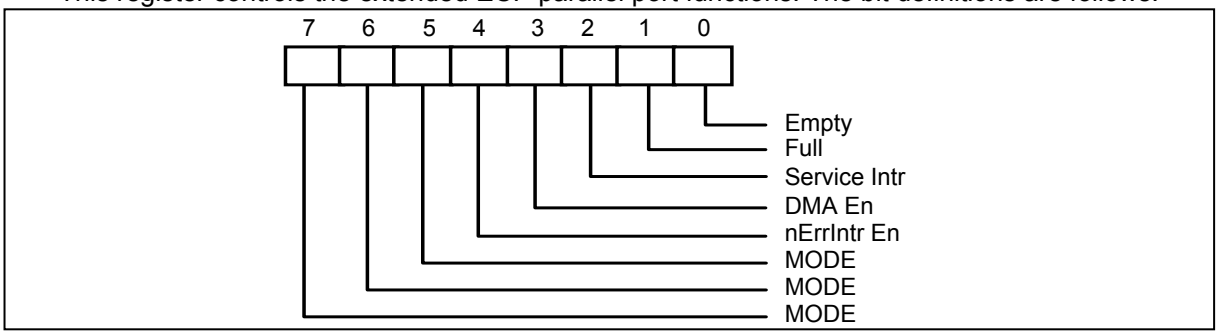
Bit 5-3: Reflect the IRQ resource assigned for ECP port.

| CNFGB[5:3] | IRQ RESOURCE |
|---|---|
| 000 | reflect other IRQ resources selected by PnP register (default) |
| 001 | IRQ7 |
| 010 | IRQ9 |
| 011 | IRQ10 |
| 100 | IRQ11 |
| 101 | IRQ14 |
| 110 | IRQ15 |
| 111 | IRQ5 |

Bit 2-0: These five bits are at high level during a read and can be written.

### 7.3.10 ecr (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:




Bit 7-5: These bits are read/write and select the mode.

| | |
|---|---|
| 000 | Standard Parallel Port mode. The FIFO is reset in this mode. |
| 001 | PS/2 Parallel Port mode. This is the same as 000 except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. |
| 010 | Parallel Port FIFO mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0. |
| 011 | ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. When the direction is 1 (reverse direction) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. |
| 100 | Selects EPP Mode. In this mode, EPP is active if the EPP supported option is selected. |
| 101 | Reserved. |
| 110 | Test Mode. The FIFO may be written and read in this mode, but the data will not be transmitted on the parallel port. |
| 111 | Configuration Mode. The confgA and confgB registers are accessible at 0x400 and 0x401 in this mode. |

Bit 4: Read/Write (Valid only in ECP Mode)

| | |
|---|---|
| 1 | Disables the interrupt generated on the asserting edge of nFault. |
| 0 | Enables an interrupt pulse on the high to low edge of nFault. If nFault is asserted (interrupt) an interrupt will be generated and this bit is written from a 1 to 0. |

Bit 3: Read/Write

| | |
|---|---|
| 1 | Enables DMA. |
| 0 | Disables DMA unconditionally. |

Bit 2: Read/Write

1 Disables DMA and all of the service interrupts.

0 Enables one of the following cases of interrupts. When one of the service interrupts has occurred, the serviceIntr bit is set to a 1 by hardware. This bit must be reset to 0 to re-enable the interrupts. Writing a 1 to this bit will not cause an interrupt.

(a) dmaEn = 1:

During DMA this bit is set to a 1 when terminal count is reached.

(b) dmaEn = 0 direction = 0:

This bit is set to 1 whenever there are writeIntr Threshold or more bytes free in the FIFO.

(c) dmaEn = 0 direction = 1:

This bit is set to 1 whenever there are readIntr Threshold or more valid bytes to be read from the FIFO.

Bit 1: Read only

0 The FIFO has at least 1 free byte.

1 The FIFO cannot accept another byte or the FIFO is completely full.

Bit 0: Read only

0 The FIFO contains at least 1 byte of data.

1 The FIFO is completely empty.

### 7.3.11 Bit Map of ECP Port Registers

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | NOTE |
|---|---|---|---|---|---|---|---|---|---|
| Data | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 | |
| ecpAFifo | Addr/RLE | Address or RLE field | | | | | | | 2 |
| Dsr | nBusy | nAck | PError | Select | nFault | 1 | 1 | 1 | 1 |
| Dcr | 1 | 1 | Directio | ackIntEn | SelectIn | nInit | autofd | strobe | 1 |
| cFifo | Parallel Port Data FIFO | | | | | | | | 2 |
| ecpDFifo | ECP Data FIFO | | | | | | | | 2 |
| tFifo | Test FIFO | | | | | | | | 2 |
| cnfgA | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | |
| cnfgB | compress | intrValue | 1 | 1 | 1 | 1 | 1 | 1 | |
| Ecr | MODE | | | nErrIntrEn | dmaEn | serviceIntr | full | empty | |

**Notes:**

1. These registers are available in all modes.

2. All FIFOs use one common 16-byte FIFO.

### 7.3.12 ECP Pin Descriptions

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| nStrobe (HostClk) | O | The nStrobe registers data or address into the slave on the asserting edge during write operations. This signal handshakes with Busy. |
| PD<7:0> | I/O | These signals contains address or data or RLE data. |
| nAck (PeriphClk) | I | This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutofd in reverse. |
| Busy (PeriphAck) | I | This signal desserts to indicate that the peripheral can accept data. It indicates whether the data lines contain ECP command information or data in the reverse direction. When in reverse direction, normal data are transferred when Busy (PeriphAck) is high and an 8-bit command is transferred when it is low. |
| PError (nAckReverse) | I | This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus. |
| Select (Xflag) | I | Indicates printer on line. |
| nAutoFd (HostAck) | O | Requests a byte of data from the peripheral when it is asserted. This signal indicates whether the data lines contain ECP address or data in the forward direction. When in forward direction, normal data are transferred when nAutoFd (HostAck) is high and an 8-bit command is transferred when it is low. |
| nFault (nPeriphRequest) | I | Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP Mode. |
| nInit (nReverseRequest) | O | This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. |
| nSelectIn (ECPMode) | O | This signal is always deasserted in ECP mode. |

### 7.3.13 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits. The following are required:

(a) Set direction = 0, enabling the drivers.

(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

(c) Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

(d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

Mode Switching

Software will execute P1284 negotiation and all operations prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can be changed only in mode 001.

When in extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001.

Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

Data Compression

The W83877TF/TG supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Note that the odd (RLE) compression in hardware is not supported. In order to transfer data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

### 7.3.14 FIFO Operation

The FIFO threshold is set in configuration register 5. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

### 7.3.15 DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or CFifo. The DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, which will disable the DMA.

### 7.3.16 Programmed I/O (NON-DMA) Mode

The ECP or parallel port FIFOs can also be operated using interrupt driven programmed I/O. Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. The host must set the direction, state, dmaEn = 0 and serviceIntr = 0 in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

## 7.4 Extension FDD Mode (EXTFDD)

In this mode, the W83877TF/TG changes the printer interface pins to FDC input/output pins, allowing the user to install a second floppy disk drive (FDD B) through the DB-25 printer connector. The pin assignments for the FDC input/output pins are shown in Table 8-1.

After the printer interface is set to EXTFDD mode, the following occur:

(1) Pins $\overline{\text{MOB}}$ and $\overline{\text{DSB}}$ will be forced to inactive state.

(2) Pins $\overline{\text{DSKCHG}}$, $\overline{\text{RDATA}}$, $\overline{\text{WP}}$, $\overline{\text{TRAK0}}$, $\overline{\text{INDEX}}$ will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.

(3) Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.

(4) If the parallel port is set to EXTFDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

## 7.5 Extension 2FDD Mode (EXT2FDD)

In this mode, the W83877TF/TG changes the printer interface pins to FDC input/output pins, allowing the user to install two external floppy disk drives through the DB-25 printer connector to replace internal floppy disk drives A and B. The pin assignments for the FDC input/output pins are shown in Table 8-1.

After the printer interface is set to EXTFDD mode, the following occur:

(1) Pins $\overline{\text{MOA}}$, $\overline{\text{DSA}}$, $\overline{\text{MOB}}$, and $\overline{\text{DSB}}$ will be forced to inactive state.

(2) Pins $\overline{\text{DSKCHG}}$, $\overline{\text{RDATA}}$, $\overline{\text{WP}}$, $\overline{\text{TRAK0}}$, and $\overline{\text{INDEX}}$ will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.

(3) Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.

(4) If the parallel port is set to EXT2FDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

# 8. PLUG AND PLAY CONFIGURATION

A powerful new plug-and-play function has been built into the W83877TF/TG to help simplify the task of setting up a computer environment. With appropriate support from BIOS manufacturers, the system designer can freely allocate Winbond I/O devices (i.e., the FDC, PRT and UART ) in the PC's I/O space (100H - 3FFH). In addition, the W83877TF/TG also provides 8 interrupt requests and 3 DMA pairs for designers to assign in interfacing FDCs, UARTs, and PRTs. Hence this powerful I/O chip offers greater flexibility for system designers.

The PnP feature is implemented through a set of Extended Function Registers (CR20 to 29). Details on configuring these registers are given in Section 11. The default values of these PnP-related registers set the system to a configuration compatible with environments designed with previous Winbond I/O chips.

# 9. ACPI /LEGACY FEATURE AND AUTO POWER MANAGEMENT

## 9.1 ACPI/Legacy power management

W83877TF/TG supports both ACPI and legacy power management models. For the ACPI power management, the $\overline{SCI}$ pin is dedicated to the SCI interrupt signal for the SCI interrupt handler; For the legacy power management, the $\overline{SMI}$ pin is dedicated to the SMI interrupt signal for the SMI interrupt handler.

Two register blocks is used for the ACPI/Legacy power management. They are the PM1 and GPE register blocks. Their base addresses are held in the W83877TF/TG configuration registers CR33 and CR34 respectively. Configuration registers CR40 to CR45 are for the legacy power management. The above configuration registers hold the interrupt event enable and status bits of the SMI interrupts. Control over the routing of SCI and SMI interrupts to the output pins is also contained in the above registers.

One 24-bit power management timer is also implemented. It provides an accurate time value used by the system software to measure and profiles system idleness.

## 9.2 Device(auto) power management

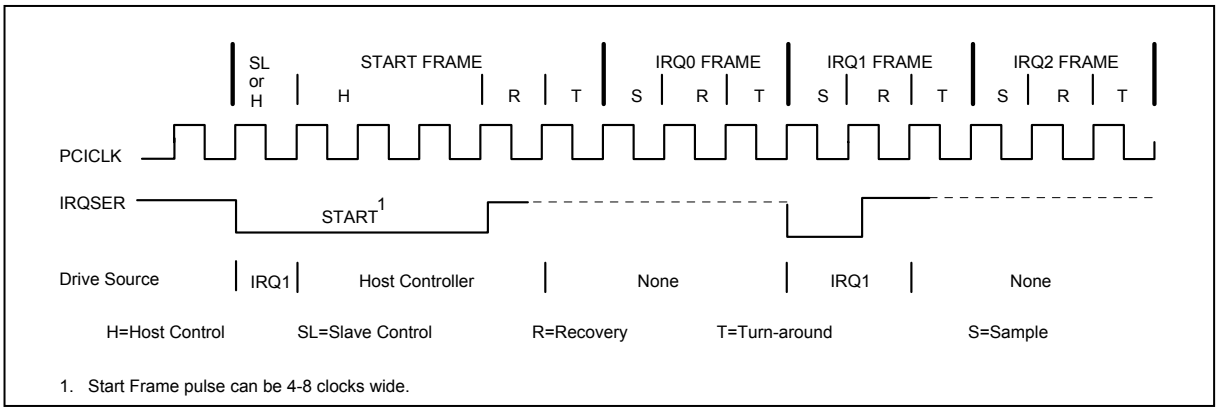
W83877TF/TG also provides the auto power management function for each device within it. They are the printer port, FDC, UART A, and UART B devices in W83877TF/TG respectively. Device idle and trap status are provided to indicate the device's working/sleeping state. Device idle timer with programmable initial value is provided for each device, which enter the powerdown state when the powerdown conditions are met. Any access to certain registers and external event input will wake up the devices. The global stand-by timer deals with the other logic part excluding the printer port, FDC, UART A , and UART B devices. The global stand-by timer reloads and counts down as soon as the 4 devices enter the powerdown mode and W83877TF/TG enters the powerdown mode as soon as it expires. Once any device is awakened, the global stand-by is also awakened. The initial count values of the devices are held in the configuration registers CR35 to CR39.

## 10. SERIAL IRQ

W83877TF/TG supports a serial IRQ scheme. This allow a signal line to be used to report the legacy ISA interrupt requests. Because more than one device may need to share the signal serial IRQ signal line, an open drain signal scheme is used. The clock source is the PCI clock. The serial interrupt is transferred on the IRQSER signal, one cycle consisting of three frames types: a start frame, several IRQ/Data frame, and one Stop frame. The serial interrupt scheme adheres to the *Serial IRQ Specification for PCI System, Version 6.0.*

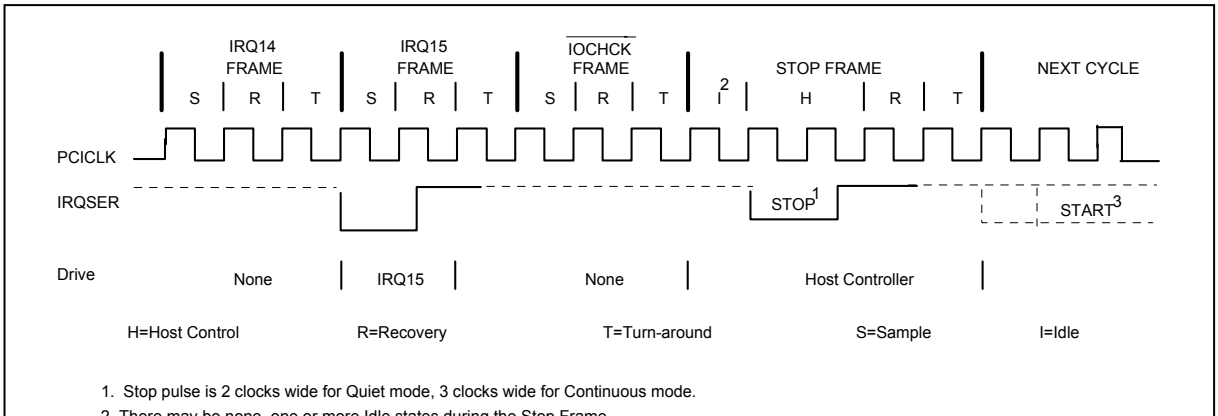
### Timing Diagrams For IRQSER Cycle

### Start Frame timing with source sampled a low pulse on IRQ1




1. Start Frame pulse can be 4-8 clocks wide.

### Stop Frame Timing with Host using 17 IRQSER sampling period




1. Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.
2. There may be none, one or more Idle states during the Stop Frame.
3. The next IRQSER cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stip Frame.

## 10.1 Start Frame

There are two modes of operation for the IRQSER Start frame: Quiet mode and Continuous mode.

In the Quiet mode, the peripheral drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the states machines of the peripherals from idle to active states. the host controller will then take over driving IRQSER signal low in the next clock and will continue driving the IRQSER low for programmable 3 to 7 clock periods. This makes the total number of clocks low for 4 to 8 clock periods. After these clocks, the host controller will drive the IRQSER high for one clock and then tri-stated.

In the Continuous mode, only the host controller initiates the START frame to update IRQ/Data line information. The host controller drives the IRQSER signal low for 4 to 8 period clocks. Upon reset, the IRQSER signal is defaulted to the Continuous mode for the host controller to initiate the first Start frame.

## 10.2 IRQ/Data Frame

Once the start frame has been initiated, all the peripherals must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase.

During the Sample phase, the peripheral drives SERIRQ low if the corresponding IRQ should be active. If the corresponding IRQ is inactive, then IRQSER must be left tri-stated. During the Recovery phase, the peripheral device drives the IRQSER high. During the Turn-around phase, the peripheral device left the IRQSER tri-stated.

The IRQ/Data Frame has a number of specific order, as shown in Table 10-1.

Table 10-1 IRQSER Sampling periods

| IRQ/DATA FRAME | SIGNAL SAMPLED | # OF CLOCKS PAST START |
|---|---|---|
| 1 | IRQ0 | 2 |
| 2 | IRQ1 | 5 |
| 3 | $\overline{\text{SMI}}$ | 8 |
| 4 | IRQ3 | 11 |
| 5 | IRQ4 | 14 |
| 6 | IRQ5 | 17 |
| 7 | IRQ6 | 20 |
| 8 | IRQ7 | 23 |
| 9 | IRQ8 | 26 |
| 10 | IRQ9 | 29 |
| 11 | IRQ10 | 32 |
| 12 | IRQ11 | 35 |
| 13 | IRQ12 | 38 |
| 14 | IRQ13 | 41 |

IRQ/Data Frame, continued

| IRQ/DATA FRAME | SIGNAL SAMPLED | # OF CLOCKS PAST START |
|---|---|---|
| 15 | IRQ14 | 44 |
| 16 | IRQ15 | 47 |
| 17 | $\overline{\text{IOCHCK}}$ | 50 |
| 18 | $\overline{\text{INTA}}$ | 53 |
| 19 | $\overline{\text{INTB}}$ | 56 |
| 20 | $\overline{\text{INTC}}$ | 59 |
| 21 | $\overline{\text{INTD}}$ | 62 |
| 32:22 | Unassigned | 95 |

## 10.3 Stop Frame

After all IRQ/Data Frames have completed , the host controller will terminate IRQSER by a Stop frame. Only the host controller can initiate the Stop frame by driving IRQSER low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the next IRQSER cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the next IRQSER cycle's Sample mode is the Continuous mode.

## 10.4 Reset and Initialization

After MR reset, IRQSER Slaves are put into the Continuous(Idle) mode. The Host Controller is responsible for starting the initial IRQSER Cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent IRQSER cycles. It's the Host Controller's responsibility to provide the default values to 8259's and other system logic before the first IRQSER cycle is performed. For IRQSER system suspend, insertion, or removal application, the Host controller should be programmed into Continuous(Idle) mode first. This is to guarantee IRQSER bus in the Idle state before the system configuration changes.

# 11. EXTENDED FUNCTION REGISTERS

The W83877TF/TG provides many configuration registers for setting up different types of configurations. After power-on reset, the state of the hardware setting of each pin will be latched by the relevant configuration register to allow the W83877TF/TG to enter the proper operating configuration. To protect the chip from invalid reads or writes, the configuration registers cannot be accessed by the user. There are four ways to enable the configuration.

n registers to be read or written. HEFERE (CR0C bit 5) and HEFRAS (CR16 bit 0) can be used to select one out of these four methods of entering the Extended Function mode as follows:

| HEFRAS | HEFERE | ADDRESS AND VALUE |
|---|---|---|
| 0 | 0 | write 88H to the location 250H |
| 0 | 1 | write 89H to the location 250H (power-on default) |
| 1 | 0 | write 86H to the location 3F0H twice |
| 1 | 1 | write 87H to the location 3F0H twice |

First, a specific value must be written once (88H/89H) or twice (86H/87H) to the Extended Functions Enable Register (I/O port address 250H or 3F0H). Second, an index value (00H-19H, 20H-29H, 2CH-2DH, 31H-3AH, 40H-45H) must be written to the Extended Functions Index Register (I/O port address 251H or 3F0H) to identify which configuration register is to be accessed. The designer can then access the desired configuration register through the Extended Functions Data Register (I/O port address 252H or 3F1H).

After programming of the configuration register is finished, an additional value should be written to EFERs to exit the Extended Function mode to prevent unintentional access to those configuration registers. In the case of EFER at 250H, this additional value can be any value other than 88H if HEFERE = 0 and 89H if HEFERE = 1. While EFER is at 3F0H, this additional value must be AAH. The designer can also set bit 6 of CR9 (LOCKREG) to high to protect the configuration registers against accidental accesses.

The configuration registers can be reset to their default or hardware settings only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

## 11.1 Extended Functions Enable Registers (EFERs)

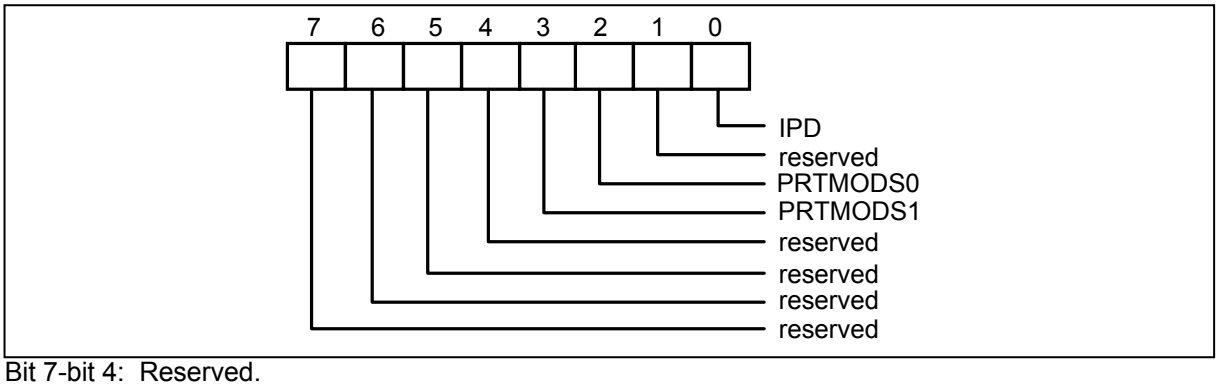
After a power-on reset, the W83877TF/TG enters the default operating mode. Before the W83877TF/TG enters the extended function mode, a specific value must be programmed into the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Registers are write-only registers. On a PC/AT system, their port addresses are 250H or 3F0H (as described in the above section).

## 11.2 Extended Function Index Registers (EFIRs), Extended Function Data Registers(EFDRs)

After the extended function mode is entered, the Extended Function Index Register (EFIR) must be loaded with an index value (0H, 1H, 2H, ..., or 29H) to access Configuration Register 0 (CR0), Configuration Register 1 (CR1), Configuration Register 2 (CR2), and so forth through the Extended Function Data Register (EFDR). The EFIRs are write-only registers with port address 251H or 3F0H (as described in section 11.0) on PC/AT systems; the EFDRs are read/write registers with port address 252H or 3F1H (as described in section 11.0) on PC/AT systems. The function of each configuration register is described below.

### 11.2.1 Configuration Register 0 (CR0), default = 00H

When the device is in Extended Function mode and EFIR is 0H, the CR0 register can be accessed through EFDR. The bit definitions for CR0 are as follows:




Bit 7-bit 4: Reserved.

PRTMOD1 PRTMOD0 (Bit 3, 2):

These two bits and PRTMOD2 (CR9 bit 7) determine the parallel port mode of the W83877TF (as shown in the following Table 11-1).

Table 11-1

| PRTMODS2 (BIT 7 OF CR9) | PRTMODS1 (BIT 3 OF CR0) | PRTMODS0 (BIT 2 OF CR0) | |
|---|---|---|---|
| 0 | 0 | 0 | Normal |
| 0 | 0 | 1 | EXTFDC |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | EXT2FDD |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | EPP/SPP |
| 1 | 1 | 0 | ECP |
| 1 | 1 | 1 | ECP/EPP |

| | |
|---|---|
| 00 | Normal Mode (Default), PRTMOD2 = 0<br>Default state after power-on reset. In this mode, the W83877TF is fully compatible with the SPP and BPP mode. |
| 01 | Extension FDD Mode (EXTFDD), PRTMOD2 = 0 |
| 10 | Reserved, PRTMOD2 = 0 |
| 11 | Extension 2FDD Mode (EXT2FDD), PRTMOD2 = 0 |
| 00 | Reserved, PRTMOD2 = 1 |
| 01 | EPP Mode and SPP Mode, PRTMOD2 = 1 |
| 10 | ECP Mode, PRTMOD2 = 1 |
| 11 | ECP Mode and EPP Mode, PRTMOD2 = 1 |

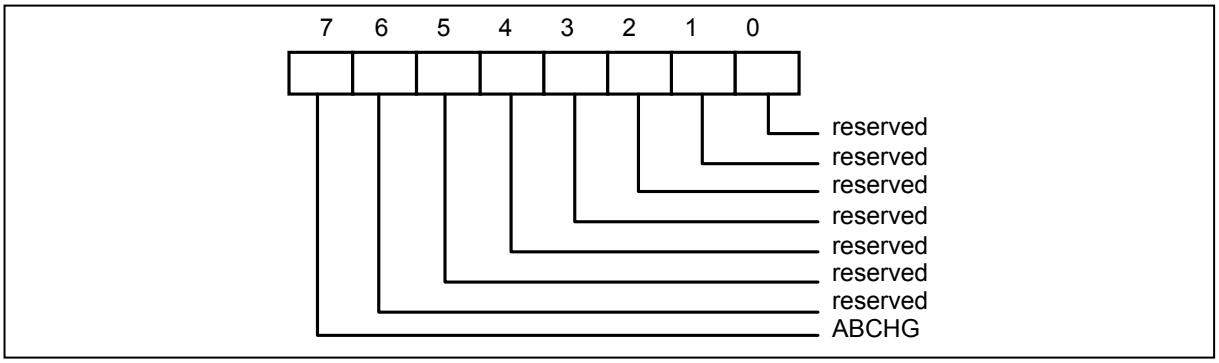
Bit 1: Reserved.

IPD (Bit 0):

This bit is used to select the W83877TF/TG's legacy power-down functions. When the bit 0 is set to 1, W83877TF/TG will stop its clock internally and enter power-down (IPD) mode immediately. W83877TF/TG will not leave the power-down mode until either a system power-on reset from the MR pin or this bit is reset to 0 to program the chip back to power-on state.

### 11.2.2 Configuration Register 1 (CR1), default = 00H

When the device is in Extended Function mode and EFIR is 01H, the CR1 register can be accessed through EFDR. The bit definitions are as follows:




ABCHG (Bit 7):

This bit enables the FDC AB Change Mode. Default to be enabled at power-on reset.

| | |
|---|---|
| 0 | Drives A and B assigned as usual |
| 1 | Drive A and drive B assignments exchanged |

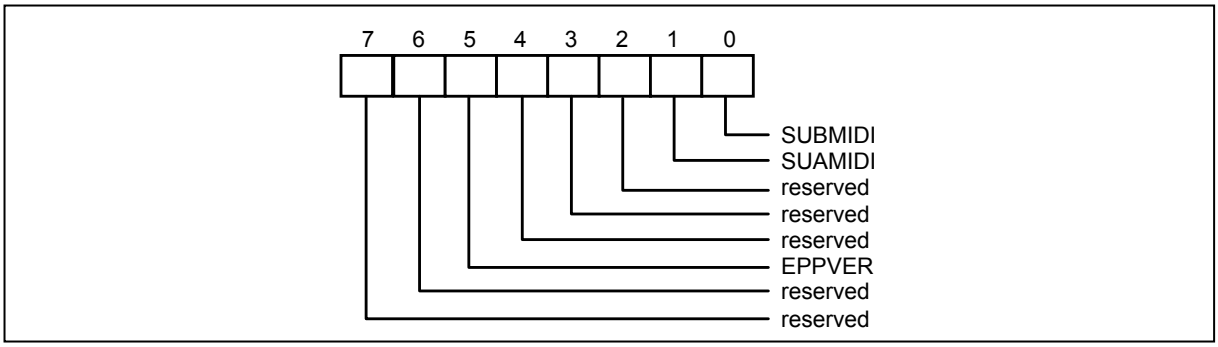
Bit 6-bit 0: Reserved.

### 11.2.3 Configuration Register 2 (CR2), default = 00H

When the device is in Extended Function mode and EFIR is 02H, the CR2 register can be accessed through EFDR. This register is reserved.

### 11.2.4 Configuration Register 3 (CR3), default = 30H

When the device is in Extended Function mode and EFIR is 03H, the CR3 register can be accessed through EFDR. The bit definitions are as follows:




Bit 7-bit 6: Reserved.

EPPVER (Bit 5):

This bit selects the EPP version of parallel port:

| | |
|---|---|
| 0 | Selects the EPP 1.9 version |
| 1 | Selects the EPP 1.7 version (default) |

Bit 4: Reserved.

Bit 3-bit 2: Reserved.

SUAMIDI (Bit 1):

This bit selects the clock divide rate of UARTA.

| | |
|---|---|
| 0 | Disables MIDI support, UARTA clock = 24 MHz divided by 13 (default) |
| 1 | Enables MIDI support, UARTA clock = 24 MHz divided by 12 |

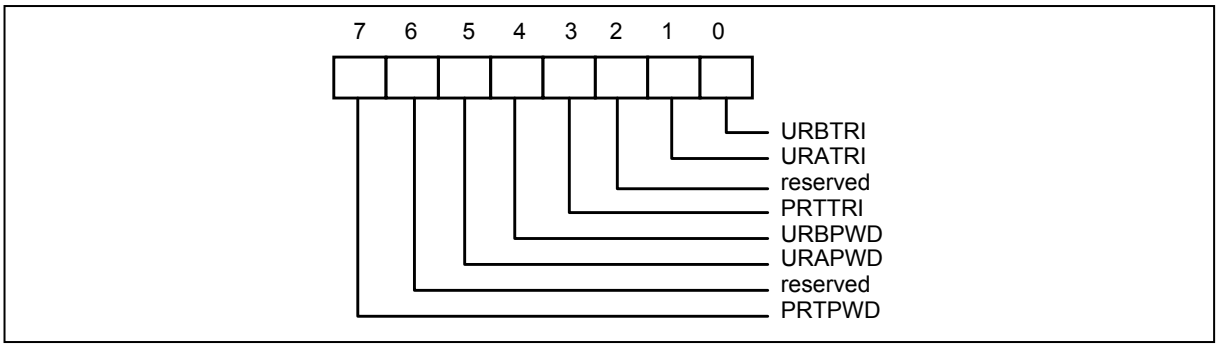
SUBMIDI (Bit 0):

This bit selects the clock divide rate of UARTB.

| | |
|---|---|
| 0 | Disables MIDI support, UARTB clock = 24 MHz divided by 13 (default) |
| 1 | Enables MIDI support, UARTB clock = 24 MHz divided by 12 |

### 11.2.5 Configuration Register 4 (CR4), default = 00H

When the device is in Extended Function mode and EFIR is 04H, the CR4 register can be accessed through EFDR. The bit definitions are as follows:




PRTPWD (Bit 7):

0 Supplies power to the parallel port (default)

1 Puts the parallel port in power-down mode

Bit 6: Reserved.

URAPWD (Bit 5):

0 Supplies power to COMA (default)

1 Puts COMA in power-down mode

URBPWD (Bit 4):

0 Supplies power to COMB (default)

1 Puts COMB in power-down mode

PRTTRI (Bit 3):

This bit enables or disables the tri-state outputs of parallel port in power-down mode.

0 The output pins of the parallel port will not be tri-stated when parallel port is in power-down mode. (default)

1 The output pins of the parallel port will be tri-stated when parallel port is in power-down mode.

Bit 2: Reserved.

URATRI (Bit 1):

This bit enables or disables the tri-state outputs of UARTA in power-down mode.

0 The output pins of UARTA will not be tri-stated when UARTA is in power-down mode.

1 The output pins of UARTA will be tri-stated when UARTA is in power-down mode.

URBTRI (Bit 0):

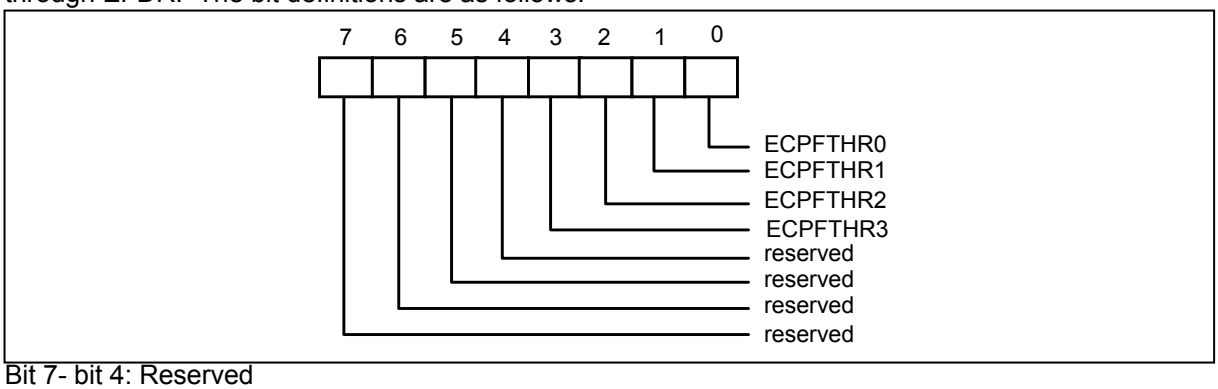
This bit enables or disables the tri-state outputs of UARTB in power-down mode.

0 The output pins of UARTB will not be tri-stated when UARTB is in power-down mode.

1 The output pins of UARTB will be tri-stated when UARTB is in power-down mode.

### 11.2.6 Configuration Register 5 (CR5), default = 00H

When the device is in Extended Function mode and EFIR is 05H, the CR5 register can be accessed through EFDR. The bit definitions are as follows:

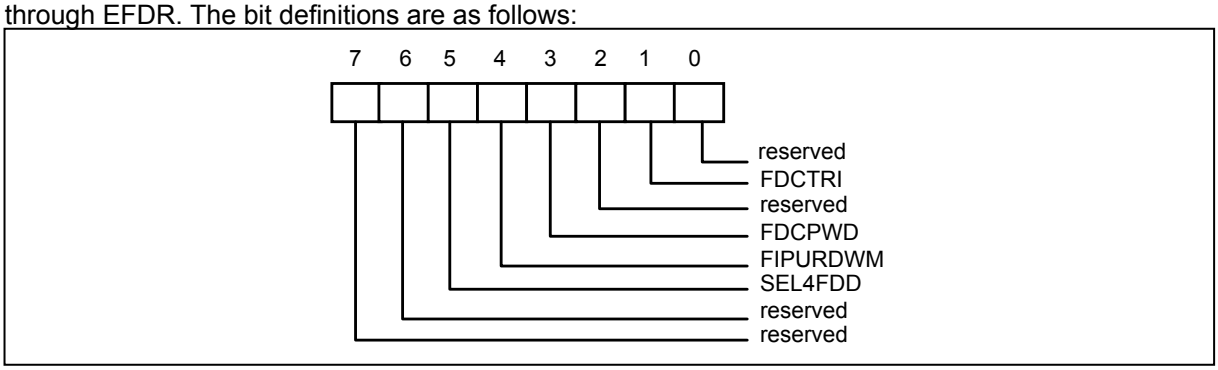



Bit 7- bit 4: Reserved

ECPFTHR3-0 (bit 3-0): These four bits define the FIFO threshold for the ECP mode parallel port. The default value is 0000 after power-up.

### 11.2.7 Configuration Register 6 (CR6), default = 00H

When the device is in Extended Function mode and EFIR is 06H, the CR6 register can be accessed through EFDR. The bit definitions are as follows:




Bit 7- bit 6: Reserved

SEL4FDD (Bit 5): Selects four FDD mode

0 Selects two FDD mode (default, see Table 11-2)

1 Selects four FDD mode

$\overline{DSA}$, $\overline{DSB}$, $\overline{MOA}$ and $\overline{MOB}$ output pins are encoded as show in Table 11-3 to select four drives.

Table 11-2

| DO REGISTER ( 3F2H ) | | | | | | $\overline{MOB}$ | $\overline{MOA}$ | $\overline{DSB}$ | $\overline{DSA}$ | DRIVE |
|---|---|---|---|---|---|---|---|---|---|---|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 1 | BIT 0 | | | | | SELECTED |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | -- |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | FDD A |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | FDD B |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | -- |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | -- |

Table 11-3

| DO REGISTER ( 3F2H ) | | | | | | $\overline{MOB}$ | $\overline{MOA}$ | $\overline{DSB}$ | $\overline{DSA}$ | DRIVE |
|---|---|---|---|---|---|---|---|---|---|---|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 1 | BIT 0 | | | | | SELECTED |
| 0 | 0 | 0 | 0 | X | X | 1 | 1 | x | x | -- |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | FDD A |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | FDD B |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | FDD C |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | FDD D |

FIPURDWN (Bit 4):

This bit controls the internal pull-up resistors of the FDC input pins $\overline{RDATA}$, $\overline{INDEX}$, $\overline{TRAK0}$, $\overline{DSKCHG}$, and $\overline{WP}$.

0 The internal pull-up resistors of FDC are turned on. (default)

1 The internal pull-up resistors of FDC are turned off.

FDCPWD (Bit 3):

This bit controls the power to the FDC.

0 Power is supplied to the FDC. (default)

1 Puts the FDC in power-down mode.

Bit 2: Reserved.

FDCTRI (Bit 1):

This bit enables or disables the tri-state outputs of the FDC in power-down mode.

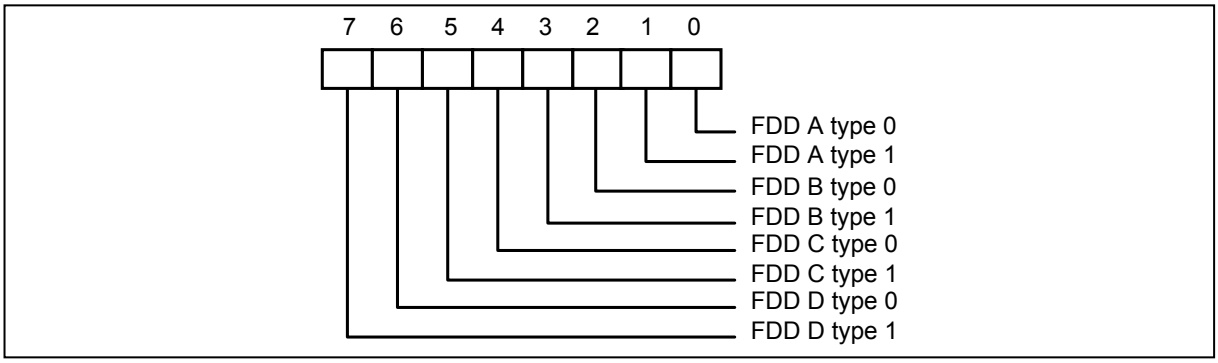
0 The output pins of the FDC will not be tri-stated when FDC is in power-down mode.

1 The output pins of the FDC will be tri-stated when FDC is in power-down mode.

Bit 0: Reserved.

### 11.2.8 Configuration Register 7 (CR7), default = 00H

When the device is in Extended Function mode and EFIR is 07H, the CR7 register can be accessed through EFDR. The bit definitions are as follows:




FDD D type 1, 0 (Bit 7, 6):

These two bits select the type of FDD D.

00 Selects normal mode. When $\overline{RWC}$ = 0, the data transfer rate is 250 Kb/s. When $\overline{RWC}$ = 1, the data transfer rate is 500 Kb/s.

Three mode FDD select (EN3MODE = 1):

01 $\overline{RWC}$ = 0, selects 1.2 MB high-density FDD.

10 $\overline{RWC}$ = 1, selects 1.44 MB high-density FDD.

11 Don't care $\overline{RWC}$, selects 720 KB double-density FDD.

FDD C type 1, 0 (Bit 5, 4):

These two bits select the type of FDD C.

00 Selects normal mode. When $\overline{RWC}$ = 0, the data transfer rate is 250 kb/s. When $\overline{RWC}$ = 1, he data transfer rate is 500 kb/s.

Three mode FDD select (EN3MODE = 1):

01 $\overline{RWC}$ = 0, selects 1.2 MB high-density FDD.

10 $\overline{RWC}$ = 1, selects 1.44 MB high-density FDD.

11 Don't care $\overline{RWC}$, selects 720 KB double-density FDD.

FDD B type 1, 0 (Bit 3, 2):

These two bits select the type of FDD B.

00 Selects normal mode. When $\overline{RWC}$ = 0, the data transfer rate is 250 Kb/s. When $\overline{RWC}$ = 1, the data transfer rate is 500 Kb/s.

Three mode FDD select (EN3MODE = 1):

01 $\overline{RWC}$ = 0, selects 1.2 MB high-density FDD.

10 $\overline{RWC}$ = 1, selects 1.44 MB high-density FDD.

11 Don't care $\overline{RWC}$, selects 720 KB double-density FDD.

FDD A type 1, 0 (Bit 1, 0):

These two bits select the type of FDD A.

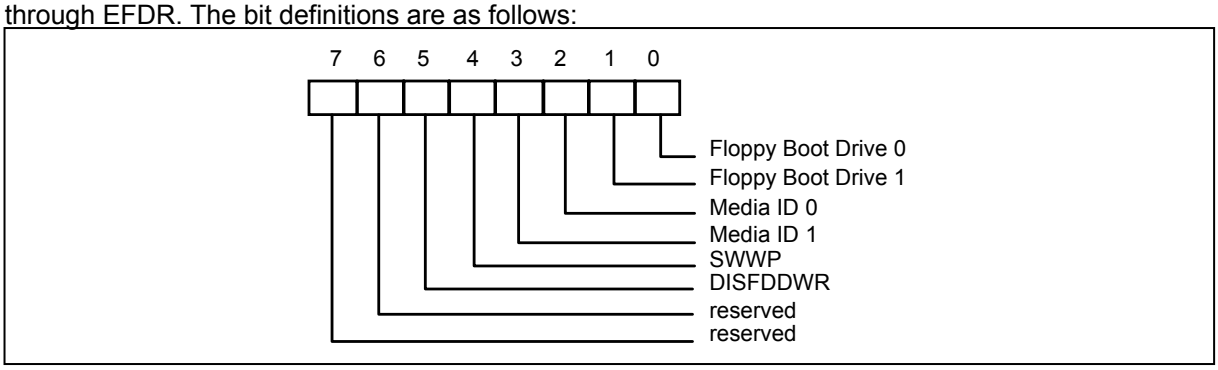
| | |
|---|---|
| 00 | Selects normal mode. When $\overline{RWC}$ = 0, the data transfer rate is 250 Kb/s. When $\overline{RWC}$ = 1, the data transfer rate is 500 Kb/s. |

Three mode FDD select (EN3MODE = 1):

| | |
|---|---|
| 01 | $\overline{RWC}$ = 0, selects 1.2 MB high-density FDD. |
| 10 | $\overline{RWC}$ = 1, selects 1.44 MB high-density FDD. |
| 11 | Don't care $\overline{RWC}$, selects 720 KB double-density FDD. |

### 11.2.9 Configuration Register 8 (CR8), default = 00H

When the device is in Extended Function mode and EFIR is 08H, the CR8 register can be accessed through EFDR. The bit definitions are as follows:




Bit 7 - bit 6: Reserved.

DISFDDWR (Bit 5):

This bit enables or disables FDD write data.

| | |
|---|---|
| 0 | Enables FDD write |
| 1 | Disables FDD write (forces pins $\overline{WE}$, $\overline{WD}$ to stay high) |

Once this bit is set high, the FDC operates normally, but because pin $\overline{WE}$ is inactive, the FDD will not write data to diskettes. For example, if a diskette is formatted with DISFDDWR = 1, after the format command has been executed, messages will be displayed that appear to indicate that the format is complete. If the diskette is removed from the disk drive and inserted again, however, typing the DIR command will reveal that the contents of the diskette have not been modified and the diskette was not actually reformatted.

Because as the operating system (e.g., DOS) reads the diskette files, it keeps the files in memory, if there is a write operation, DOS will write data to the diskette and memory simultaneously. When DOS wants to read the diskette, it will first search for the files in memory. If DOS finds the file in memory, it will not issue a read command to read the diskette. When DISFDDWR = 1, DOS still writes data to the diskette and memory, but only the data in memory are updated. If a read operation is performed, data are read from memory first, and not from the diskette. The action of removing the diskette from the drive and inserting it again forces the $\overline{DSKCHG}$ pin active. DOS will then read the contents of the

diskette and will show that the contents have not been modified. The same holds true with write commands.

This disable FDD write function allows users to protect diskettes against computer viruses by ensuring that no data are written to the diskette.

SWWP (Bit 4):

0 Normal, use $\overline{WP}$ to determine whether the FDD is write-protected or not

1 FDD is always write-protected

Media ID 1 Media ID 0 (Bit 3, 2):

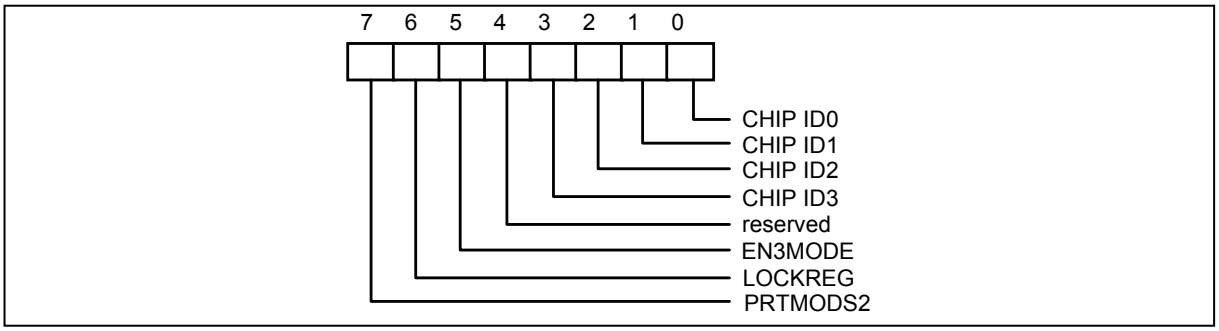
These two bits hold the media ID bit 1, 0 for three mode

Floppy Boot Drive 1 Floppy Boot Drive 0 (Bit 1, 0)

These two bits hold the value of floppy boot drive 1 and drive 0 for three mode

### 11.2.10 Configuration Register 9 (CR9), default = 0CH

When the device is in Extended Function mode and EFIR is 09H, the CR9 register can be accessed through EFDR. The bit definitions are as follows:




PRTMODS2 (Bit 7):

This bit and PRTMODS1, PRTMODS0 (bits 3, 2 of CR0) select the operating mode of the W83877TF/TG. Refer to the descriptions of CR0.

LOCKREG (Bit 6):

This bit enables or disables the reading and writing of all configuration registers.

0 Enables the reading and writing of CR0-CR45

1 Disables the reading and writing of CR0-CR45 (locks W83877TF/TG extension functions)

EN3MODE (Bit 5):

This bit enables or disables three mode FDD selection. When this bit is high, it enables the read/write 3F3H register.

0 Disables 3 mode FDD selection

1 Enables 3 mode FDD selection

When three mode FDD function is enabled, the value of $\overline{RWC}$ depends on bit 5 and bit 4 of TDR(3F3H). The values of $\overline{RWC}$ and their meaning are shown in Table 11-4.

Table 11-4

| BIT 5 OF TDR | BIT 4 OF TDR | $\overline{RWC}$ | $\overline{RWC}$ = 0 | $\overline{RWC}$ = 1 |
|---|---|---|---|---|
| 0 | 0 | Normal | 250K bps | 500K bps |
| 0 | 1 | 0 | 1.2 M FDD | X |
| 1 | 0 | 1 | X | 1.4M FDD |
| 1 | 1 | X | X | X |

Bit 4: Reserved.

CHIP ID 3, CHIP ID 2, CHIP ID 1, CHIP ID 0 (Bit 3-bit 0):

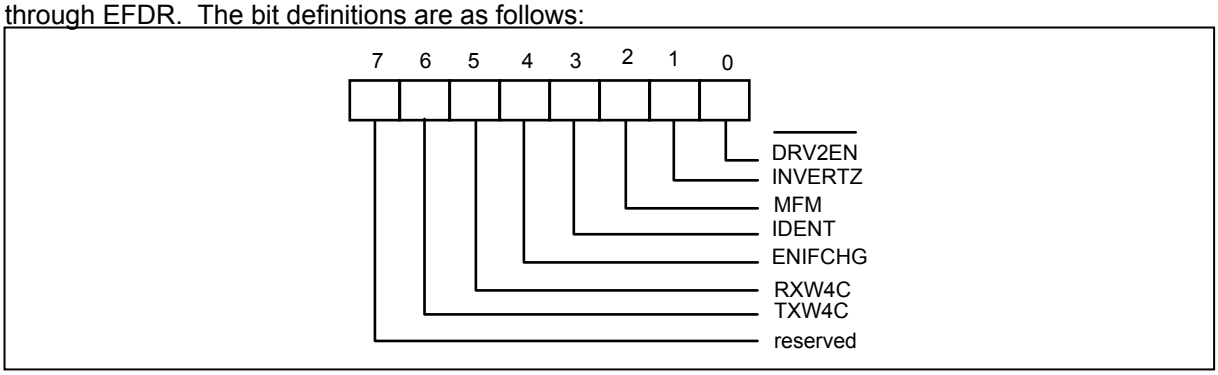
These four bits are read-only bits that contain chip identification information. The value is 0CH for W83877TF/TG during a read.

### 11.2.11 Configuration Register A (CR0A), default = 00H

When the device is in Extended Function mode and EFIR is 0AH, the CRA register can be accessed through EFDR. This register is reserved.

### 11.2.12 Configuration Register B (CR0B), default = 0CH

When the device is in Extended Function mode and EFIR is 0BH, the CRB register can be accessed through EFDR. The bit definitions are as follows:




Bit 7: Reserved.

TXW4C (Bit 6):

This bit is active high. When active, the IR controller will wait for a 4-character period of time after the end of last receiving before it can start transmitting data.

RXW4C (Bit 5):

This bit is active high. When active, the IR controller will wait for a 4-character period of time after the end of last transmitting before it can start receiving data.

ENIFCHG (Bit 4):

This bit is active high. When active, it enables host interface mode change, which is determined by IDENT (Bit 3) and MFM (Bit 2).

IDENT (Bit 3):

This bit indicates the type of drive being accessed and changes the level on $\overline{RWC}$ (pin 87).

0 $\overline{RWC}$ will be active low for high data rates (typically used for 3.5" drives)

1 $\overline{RWC}$ will be active high for high data rates (typically used for 5.25" drives)

When hardware reset or ENIFCHG is a logic 1, IDENT and MFM select one of three interface modes, as shown in Table 11-5.

Table 11-5

| IDENT | MFM | INTERFACE |
|---|---|---|
| 0 | 0 | Model 30 mode |
| 0 | 1 | PS/2 mode |
| 1 | 0 | AT mode |
| 1 | 1 | AT mode |

MFM (Bit 2):

This bit and IDENT select one of the three interface modes (PS/2 mode, Model 30, or PC/AT mode).

INTVERTZ (Bit 1):

This bit determines the polarity of all FDD interface signals.

0 FDD interface signals are active low

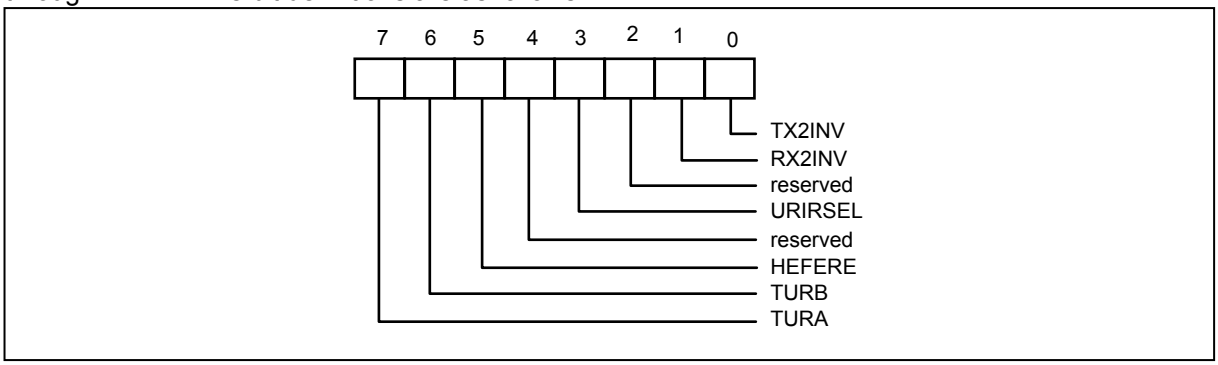
1 FDD interface signals are active high

$\overline{DRV2EN}$ (Bit 0): PS/2 mode only

When this bit is a logic 0, this indicates that a second drive is installed and is reflected in status register A.

### 11.2.13 Configuration Register C (CR0C), default = 28H

When the device is in Extended Function mode and EFIR is 0CH, the CR0C register can be accessed through EFDR. The bit definitions are as follows:



TURA (Bit 7):

0 the clock source of UART A is 1.8462 MHZ (24 MHz divide 13) (default)

1 the clock source of UART A is 24 MHz, it can make the baudrate of UART A up to 1.5 MHz

TURB (Bit 6):

0 the clock source of UART B is 1.8462 MHz (24 MHz divide 13) (default)

1 the clock source of UART B is 24 MHz, it can make the baudrate of UART A up to 1.5 MHz

HEFERE (Bit 5): this bit combines with HEFRAS (CR16 bit 0) to define how to enable Extended Function Registers.

| HEFRAS | HEFERE | ADDRESS AND VALUE |
|---|---|---|
| 0 | 0 | write 88H to the location 250H |
| 0 | 1 | write 89H to the location 250H (default) |
| 1 | 0 | write 86H to the location 3F0H twice |
| 1 | 1 | write 87H to the location 3F0H twice |

The default value of HEFERE is 1.

Bit 4: Reserved.

URIRSEL (Bit 3):

0 select UART B as IR function.

1 select UART B as normal function.

The default value of URIRSEL is 1.

Bit 2: Reserved.

RX2INV (Bit 1):

0 the SINB pin of UART B function or IRRX pin of IR function in normal condition.

1 inverse the SINB pin of UART B function or IRRX pin of IR function

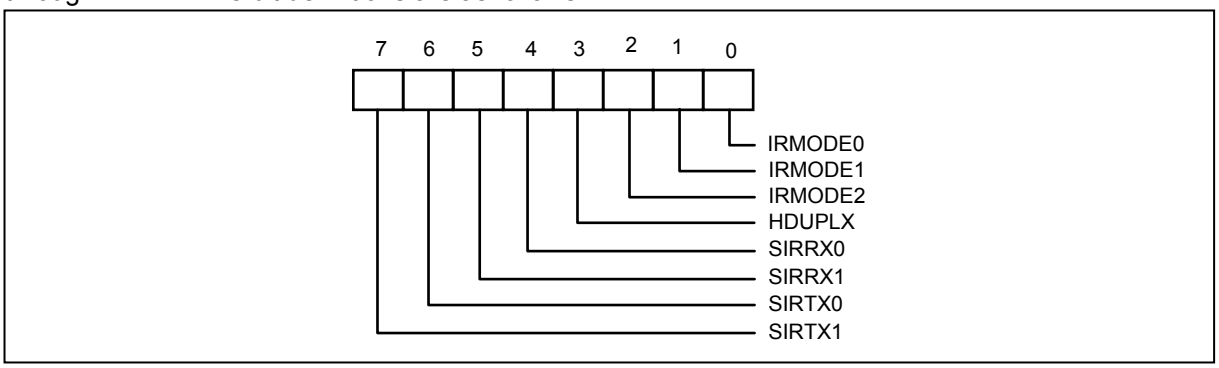
TX2INV (Bit 0):

0 the SOUTB pin of UART B function or IRTX pin of IR function in normal condition.

1 inverse the SOUTB pin of UART B function or IRTX pin of IR function.

### 11.2.14 Configuration Register D (CR0D), default = A3H

When the device is in Extended Function mode and EFIR is 0DH, the CR0D register can be accessed through EFDR. The bit definitions are as follows:




SIRTX1 (Bit 7): IRTX pin selection bit 1

SIRTX0 (Bit 6): IRTX pin selection bit 0

| SIRTX1 | SIRTX0 | IRTX OUTPUT ON PIN |
|---|---|---|
| 0 | 0 | disabled |
| 0 | 1 | IRTX1 (pin 43) |
| 1 | 0 | IRTX2 (pin 95) |
| 1 | 1 | disabled |

SIRRX1 (Bit 5): IRRX pin selection bit 1

SIRRX0 (Bit 4): IRRX pin selection bit 0

| SIRRX1 | SIRRX0 | IRRX INPUT ON PIN |
|---|---|---|
| 0 | 0 | disabled |
| 0 | 1 | IRRX1 (pin 42) |
| 1 | 0 | IRRX2 (pin 94) |
| 1 | 1 | disabled |

HDUPLX (Bit 3):

0 The IR function is Full Duplex.

1 The IR function is Half Duplex.

IRMODE2 (Bit 2): IR function mode selection bit 2

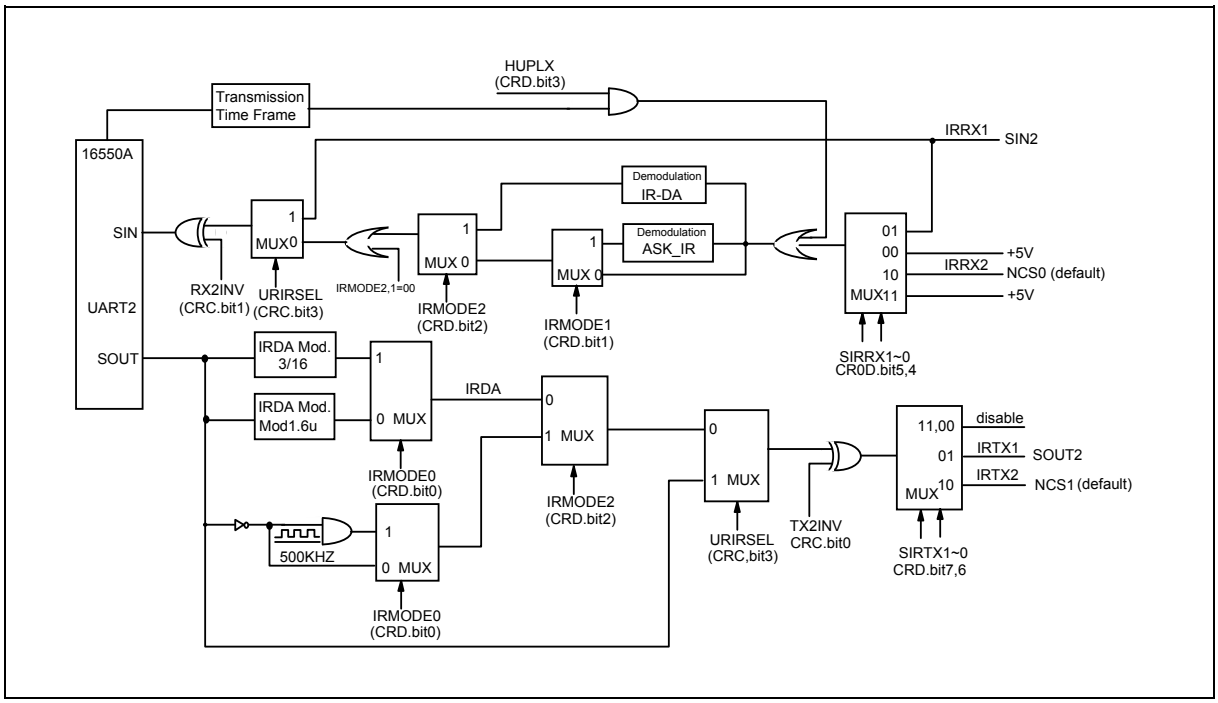
IRMODE1 (Bit 1): IR function mode selection bit 1

IRMODE0 (Bit 0): IR function mode selection bit 0

| IR MODE | IR FUNCTION | IRTX | IRRX |
|---|---|---|---|
| 00X | Disable | tri-state | high |
| 010* | IrDA | Active pulse 1.6 μS | Demodulation into SINB |
| 011* | IrDA | Active pulse 3/16 bit time | Demodulation into SINB |
| 100 | ASK-IR | Inverting IRTX pin | routed to SINB |
| 101 | ASK-IR | Inverting IRTX & 500 KHZ clock | routed to SINB |
| 110 | ASK-IR | Inverting IRTX | Demodulation into SINB |
| 111* | ASK-IR | Inverting IRTX & 500 KHZ clock | Demodulation into SINB |

**Note:** The notation is normal mode in the IR function.

The SIR schematic diagram for registers CRC and CRD is shown below.

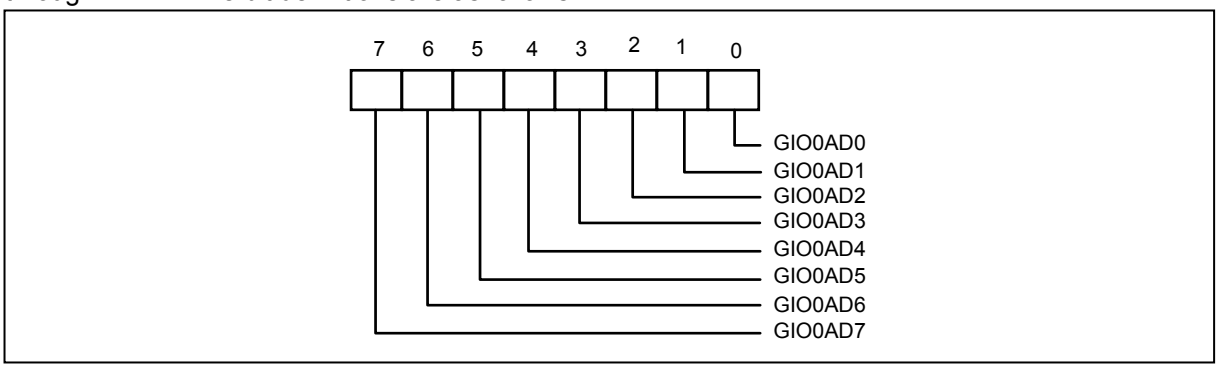



### 11.2.15 Configuration Register E (CR0E), Configuration Register F (CR0F)

Reserved for testing. Should be kept all 0's.

### 11.2.16 Configuration Register 10 (CR10), default = 00H

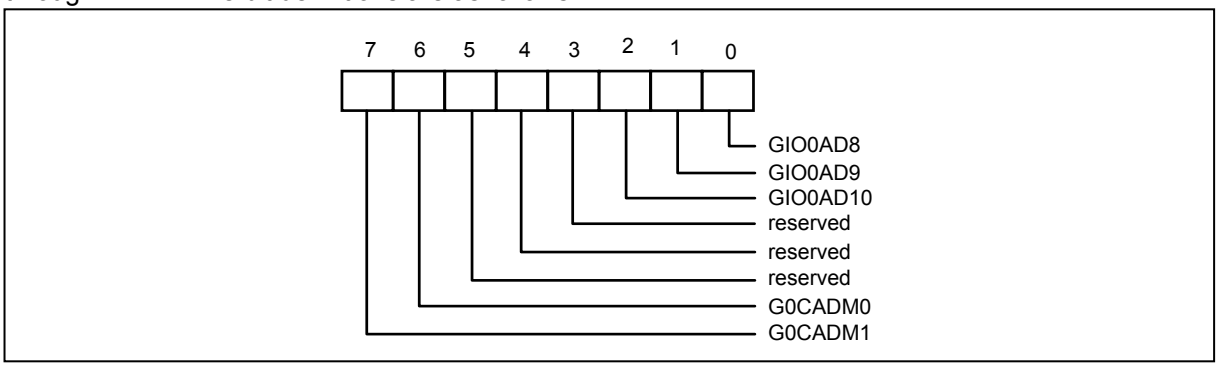
When the device is in Extended Function mode and EFIR is 10H, the CR10 register can be accessed through EFDR. The bit definitions are as follows:




GIO0AD7-GIO0AD0 (Bit 7-bit 0): GIOP0 (pin 92) address bit 7 - bit 0.

### 11.2.17 Configuration Register 11 (CR11), default = 00H

When the device is in Extended Function mode and EFIR is 11H, the CR11 register can be accessed through EFDR. The bit definitions are as follows:




G0CADM1-G0CADM0 (Bit 7, 6): GIOP0 address bit compare mode selection

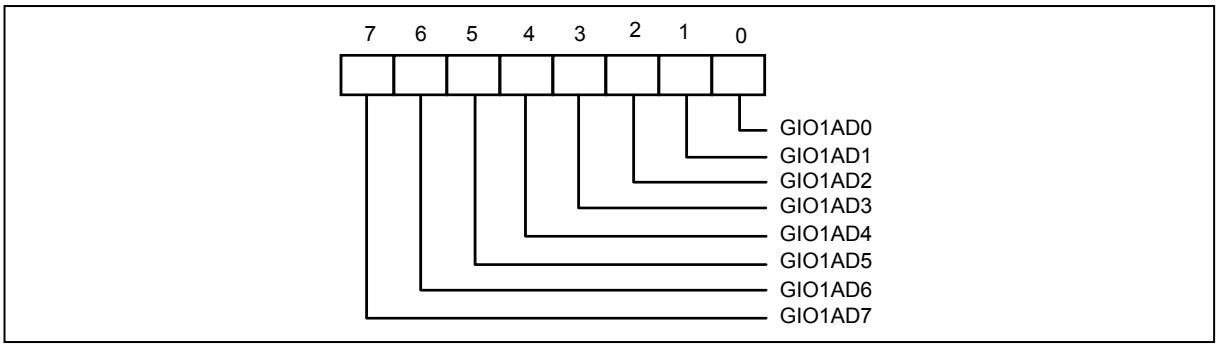
| G0CADM1 | G0CADM0 | GIOP0 PIN |
|---|---|---|
| 0 | 0 | compare GIO0AD10-GIO0AD0 with SA10-SA0 |
| 0 | 1 | compare GIO0AD10-GIO0AD1 with SA10-SA1 |
| 1 | 0 | compare GIO0AD10-GIO0AD2 with SA10-SA2 |
| 1 | 1 | compare GIO0AD10-GIO0AD3 with SA10-SA3 |

Bit 5-bit 3: Reserved

GIO0AD10-GIO0AD8 (Bit 2-bit 0): GIOP0 (pin 92) address bit 10-bit 8.

### 11.2.18 Configuration Register 12 (CR12), default = 00H

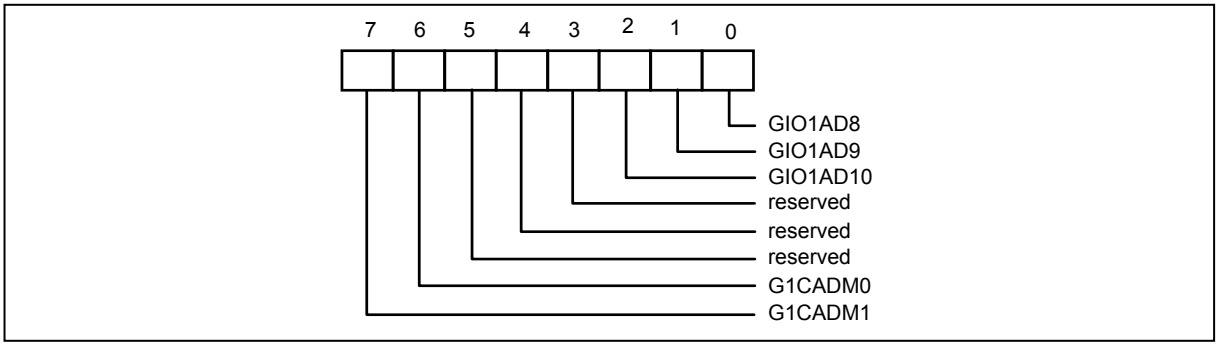
When the device is in Extended Function mode and EFIR is 12H, the CR12 register can be accessed through EFDR. The bit definitions are as follows:




GIO1AD7-GIO1AD0 (Bit 7-bit 0): GIOP1 (pin 96) address bit 7-bit 0.

### 11.2.19 Configuration Register 13 (CR13), default = 00H

When the device is in Extended Function mode and EFIR is 13H, the CR13 register can be accessed through EFDR. The bit definitions are as follows:




G1CADM1-G1CADM0 (bit 7, 6): GIOP1 address bit compare mode selection

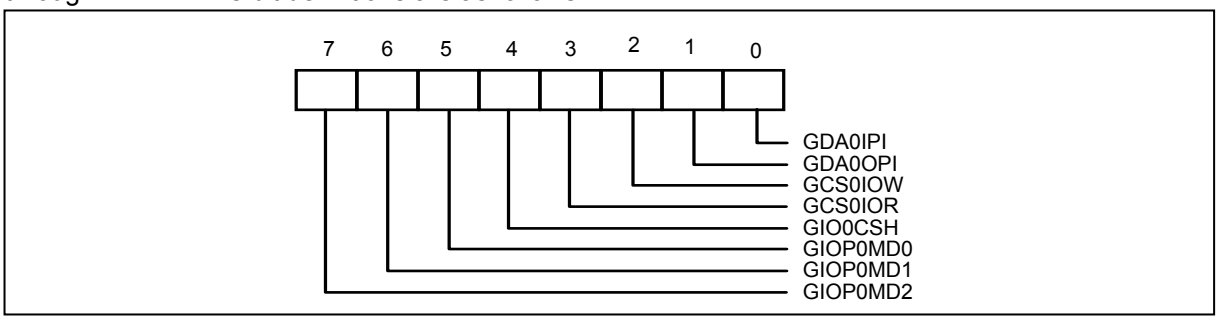
| G1CADM1 | G1CADM0 | GIOP1 PIN |
|---|---|---|
| 0 | 0 | compare GIO1AD10-GIO1AD0 with SA10-SA0 |
| 0 | 1 | compare GIO1AD10-GIO1AD1 with SA10-SA1 |
| 1 | 0 | compare GIO1AD10-GIO1AD2 with SA10-SA2 |
| 1 | 1 | compare GIO1AD10-GIO1AD3 with SA10-SA3 |

Bit 5- bit 3: Reserved

GIO1AD10-GIO1AD8 (Bit 2-bit 0): GIOP1 (pin 96) address bit 10-bit 8.

### 11.2.20 Configuration Register 14 (CR14), default = 00H

When the device is in Extended Function mode and EFIR is 14H, the CR14 register can be accessed through EFDR. The bit definitions are as follows:




GIOP0MD2-GIOP0MD0 (Bit 7-bit 5): GIOP0 pin mode selection

| GIOP0MD2 | GIOP0MD1 | GIOP0MD0 | GIOP0 PIN |
|---|---|---|---|
| 0 | 0 | 0 | inactive (tri-state) |
| 0 | 0 | 1 | as a data output pin (SD0→GIOP0), when (AEN = L) AND (NIOW = L) AND (SA10-0 = GIO0AD10-0), the value of SD0 will be present on GIOP0 |
| 0 | 1 | 0 | as a data input pin (GIOP0→SD0), when (AEN = L) AND (NIOR = L) AND (SA10-0 = GIO0AD10-0), the value of GIOP0 will be present on SD0 |
| 0 | 1 | 1 | as a data input/output pin (GIOP0↔SD0).<br>When (AEN = L) AND (NIOW = L) AND (SA10-0 = GIO0AD10-0), the value of SD0 will be present on GIOP0 When (AEN = L) AND (NIOR = L) AND (SA10-0 = GIO0AD10-0), the value of GIOP0 will be present on SD0 |
| 1 | X | X | as a Chip Select pin, the pin will be active at (AEN = L) AND (SA10-0 = GIO0AD10-0) OR (NIOR = L) OR (NIOW = L) |

GIO0CSH(Bit 4):

| | |
|---|---|
| 0 | the Chip Select pin will be active LOW when (AEN = L) AND (SA10-0 = GIO0AD10-0) OR (NIOR = L) OR (NIOW = L) |
| 1 | the Chip Select pin will be active HIGH when (AEN = L) AND (SA10-0 = GIO0AD10-0) OR (NIOR = L) OR (NIOW = L) |

GCS0IOR (Bit 3): See below.

GCS0IOW (Bit 2): See below.

| GCS0IOR | GCS0IOW | |
|---|---|---|
| 0 | 0 | GIOP0 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO0AD10-0) |
| 0 | 1 | GIOP0 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO0AD10-0) AND (NIOW = L) |
| 1 | 0 | GIOP0 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO0AD10-0) AND (NIOR = L) |
| 1 | 1 | GIOP0 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO0AD10-0) AND (NIOW = L OR NIOR = L) |

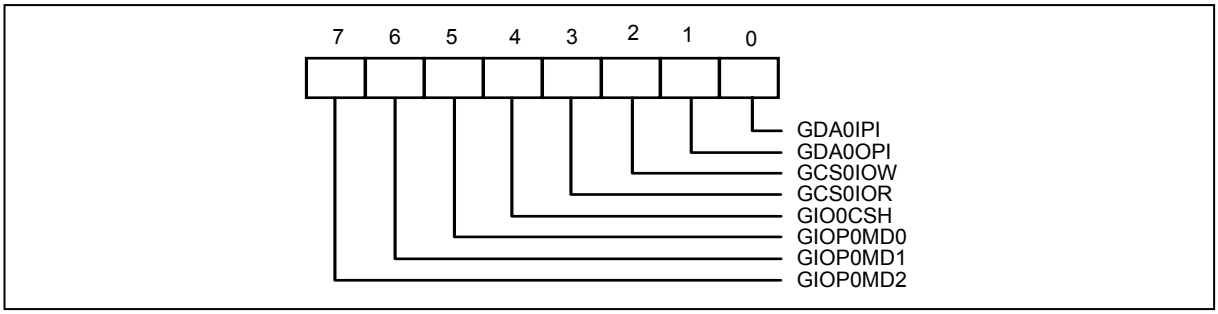
GDA0OPI (Bit 1): See below.

GDA0IPI (Bit 0): See below.

| GDA0OPI | GDA0IPI | |
|---|---|---|
| 0 | 0 | GIOP0 functions as a data pin, and GIOP0→SD0, SD0→GIOP0 |
| 0 | 1 | GIOP0 functions as a data pin, and inverse GIOP0→SD0, SD0→ GIOP0 |
| 1 | 0 | GIOP0 functions as a data pin, and GIOP0→SD0, inverse SD0→ GIOP0 |
| 1 | 1 | GIOP0 functions as a data pin, and inverse GIOP0→SD0, inverse SD0 →GIOP0 |

### 11.2.21 Configuration Register 15 (CR15), default = 00H

When the device is in Extended Function mode and EFIR is 15H, the CR15 register can be accessed through EFDR. The bit definitions are as follows:



GIOP1MD2-GIOP1MD0 (Bit 7-bit 5): GIOP1 pin mode selection

| GIOP1MD2 | GIOP1MD1 | GIOP1MD0 | GIOP1 PIN |
|---|---|---|---|
| 0 | 0 | 0 | inactive (tri-state) |
| 0 | 0 | 1 | as a data output pin (SD1→GIOP1), when (AEN = L) AND (NIOW = L) AND (SA10-0 = GIO1AD10-0), the value of SD1 will be present on GIOP1 |
| 0 | 1 | 0 | as a data input pin (GIOP1→SD1), when (AEN = L) AND (NIOR = L) AND (SA10-0 = GIO1AD10-0), the value of GIOP1 will be present on SD1 |
| 0 | 1 | 1 | as a data input/output pin (GIOP1↔SD1). When (AEN = L) AND (NIOW = L) AND (SA10-0 = GIO1AD10-0), the value of SD1 will be present on GIOP1 When (AEN = L) AND (NIOR = L) AND (SA10-0 = GIO1AD10-0), the value of GIOP1 will be present on SD1 |
| 1 | X | X | as a Chip Select pin, the pin will be active at (AEN = L) AND (SA10-0 = GIO1AD10-0) OR (NIOR = L) OR (NIOW = L) |

GIO1CSH (Bit 4):

| | |
|---|---|
| 0 | the Chip Select pin will active LOW when (AEN = L) AND (SA10-0 = GIOAD10-0) OR (NIOR = L) OR (NIOW = L) |
| 1 | the Chip Select pin will active HIGH when (AEN = L) AND (SA10-0 = GIOAD10-0) OR (NIOR = L) OR (NIOW = L) |

GCS1IOR (Bit 3): See below.

GCS1IOW (Bit 2): See below.

| GCS1IOR | GCS1IOW | |
|---|---|---|
| 0 | 0 | GIOP1 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO1AD10-0) |
| 0 | 1 | GIOP1 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO1AD10-0) AND (NIOW = L) |
| 1 | 0 | GIOP1 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO1AD10-0) AND (NIOR = L) |
| 1 | 1 | GIOP1 functions as a Chip Select pin, and will be active when (AEN = L) AND (SA10-0 = GIO1AD10-0) AND (NIOW = L OR NIOR = L) |

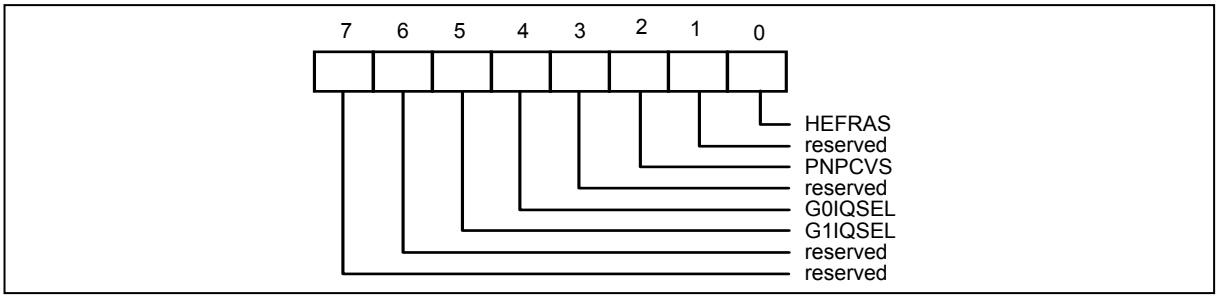
GDA0OPI (Bit 1): See below.

GDA1IPI (Bit 0): See below.

| GDA1OPI | GDA1IPI | |
|---|---|---|
| 0 | 0 | GIOP1 functions as a data pin, and GIOP1→SD1, SD1→GIOP1 |
| 0 | 1 | GIOP1 functions as a data pin, and inverse GIOP1→SD1, SD1→ GIOP1 |
| 1 | 0 | GIOP1 functions as a data pin, and GIOP1→SD1, inverse SD1→ GIOP1 |
| 1 | 1 | GIOP1 functions as a data pin, and inverse GIOP1→ SD1, inverse SD1→GIOP1 |

### 11.2.22 Configuration Register 16 (CR16), default = 04H

When the device is in Extended Function mode and EFIR is 16H, the CR16 register can be accessed through EFDR. The bit definitions are as follows:




Bit 7-bit 6: Reserved.

G1IQSEL (Bit 5):

| | |
|---|---|
| 0 | pin 96 function as IRQ_A. |
| 1 | pin 96 function as GIO1. |

The corresponding power-on setting pin is NRTSB (pin 45).

G0IQSEL (Bit 4):

| | |
|---|---|
| 0 | pins 92 function as IRQ_B. |
| 1 | pins 92 function as GIO0. |

The corresponding power-on setting pin is NRTSB (pin 45).

Bit 3: Reserved.

PNPCVS (bit 2):

| | |
|---|---|
| 0 | PnP-related registers (CR20, CR23-29) reset to be all 0s. |
| 1 | default settings for these registers. |

The corresponding power-on setting pin is NRTSA (pin 36).

| PNP REGISTER | PNPCVS = 1 | PNPCVS = 0 |
|---|---|---|
| CR20 | FCH | 00H |
| CR23 | DEH | 00H |
| CR24 | FEH | 00H |
| CR25 | BEH | 00H |
| CR26 | 23H | 00H |
| CR27 | 05H | 00H |
| CR28 | 43H | 00H |
| CR29 | 60H | 00H |

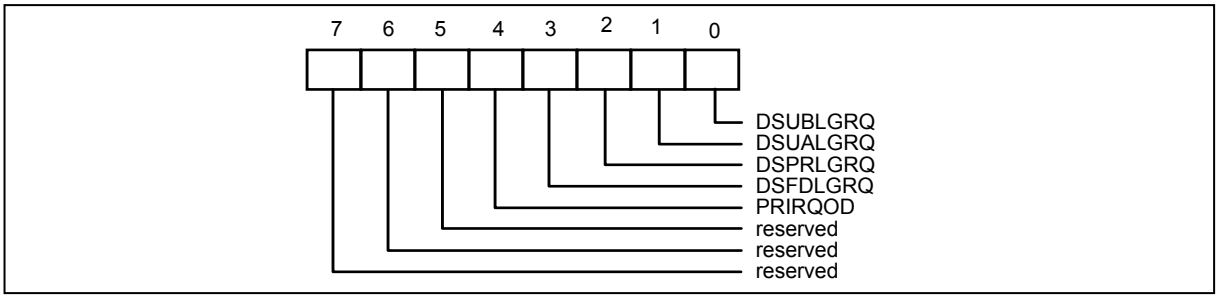
**Note:** The new value of PNPCVS must be complementary to the old one to make an effective change. For example, the user must set PNPCVS to 1 first and then reset it to 0 to reset these PnP registers if the present value of PNPCVS is 0.

Bit 1: Reserved.

HEFRAS (Bit 0): combines with HEFERE (bit 5 of CR0C) to define how to access Extended Function Registers (refer to bit 5 of CR0C description). The corresponding power-on setting pin is NDTRA (pin 35).

### 11.2.23 Configuration Register 17 (CR17), default = 00H

When the device is in Extended Function mode and EFIR is 17H, the CR17 register can be accessed through EFDR. The bit definitions are as follows:




Bit 7-bit 5: Reserved.

PRIRQOD (Bit 4):

| | |
|---|---|
| 0 | printer IRQ ports are totem-poles in SPP mode and open-drains in ECP/EPP mode. |
| 1 | printer IRQ ports are totem-poles in all modes. |

DSFDLGRQ (Bit 3):

| | |
|---|---|
| 0 | enable FDC legacy mode on IRQ and DRQ selections. DO register bit 3 has effect on selecting IRQ. |
| 1 | disable FDC legacy mode on IRQ and DRQ selections. DO register bit 3 has no effect on selecting IRQ. |

DSPRLGRQ (Bit 2):

| | |
|---|---|
| 0 | enable PRT legacy mode on IRQ and DRQ selections. DCR bit 4 has effect on selecting IRQ. |
| 1 | disable PRT legacy mode on IRQ and DRQ selections. DCR bit 4 has no effect on selecting IRQ. |

DSUALGRQ (Bit 1):

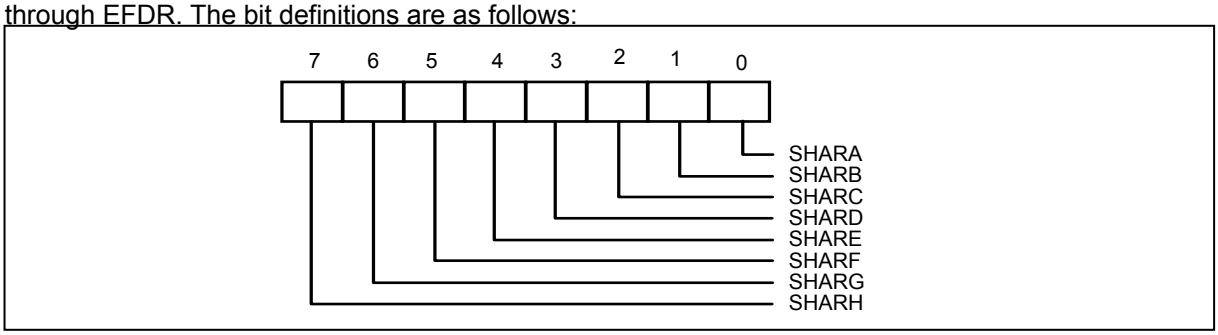
| | |
|---|---|
| 0 | enable UART A legacy mode on IRQ selection. MCR bit 3 has effect on selecting IRQ. |
| 1 | disable UART A legacy mode on IRQ selection. MCR bit 3 has no effect on selecting IRQ. |

DSUBLGRQ (Bit 0):

| | |
|---|---|
| 0 | enable UART B legacy mode on IRQ selection. MCR bit 3 has effect on selecting IRQ. |
| 1 | disable UART B legacy mode on IRQ selection. MCR bit 3 has no effect on selecting IRQ. |

### 11.2.24 Configuration Register 18 (CR18), default=00H

When the device is in Extended Function mode and EFIR is 18H, the CR18 register can be accessed through EFDR. The bit definitions are as follows:




This register is used to select whether these interrupt request pins are in the IRQ sharing mode. While in the IRQ sharing mode, the corresponding pin is low active for 200ns for the interrupt request and keeps tri-stated otherwise.

SHARH (Bit 7):

| | |
|---|---|
| 0 | pin IRQ_H in the legacy ISA IRQ mode. |
| 1 | pin IRQ_H in the IRQ sharing mode. |

SHARG (Bit 6):

| | |
|---|---|
| 0 | pin IRQ_G in the legacy ISA IRQ mode. |
| 1 | pin IRQ_G in the IRQ sharing mode. |

SHARF (Bit 5):

| | |
|---|---|
| 0 | pin IRQ_F in the legacy ISA IRQ mode. |
| 1 | pin IRQ_F in the IRQ sharing mode. |

SHARE (Bit 4):

| | |
|---|---|
| 0 | pin IRQ_E in the legacy ISA interrupt mode. |
| 1 | pin IRQ_E in the IRQ sharing mode. |

SHARD (Bit 3):

| | |
|---|---|
| 0 | pin IRQ_D in the legacy ISA IRQ mode. |
| 1 | pin IRQ_D in the IRQ sharing mode. |

SHARC (Bit 2):

| | |
|---|---|
| 0 | pin IRQ_C in the legacy ISA IRQ mode. |
| 1 | pin IRQ_C in the IRQ sharing mode. |

SHARB(Bit 1):

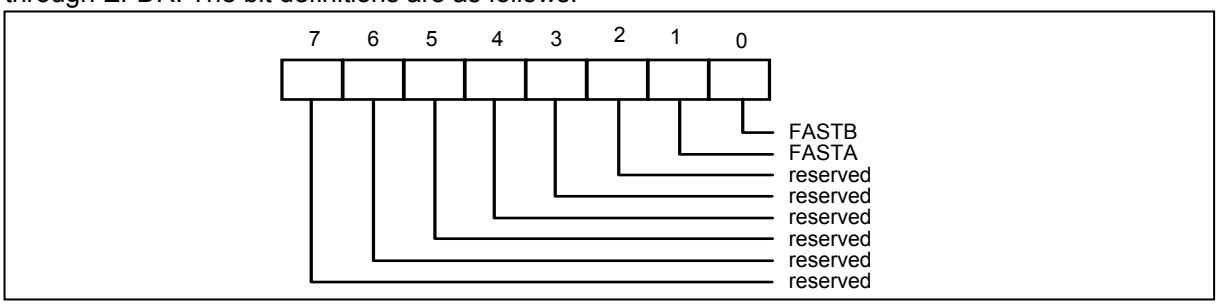
| | |
|---|---|
| 0 | pin IRQ_B in the legacy ISA IRQ mode. |
| 1 | pin IRQ_B in the IRQ sharing mode. |

SHARA (Bit 0):

| | |
|---|---|
| 0 | pin IRQ_A in the legacy ISA IRQ mode. |
| 1 | pin IRQ_A in the IRQ sharing mode. |

### 11.2.25 Configuration Register 19 (CR19), default=00H

When the device is in Extended Function mode and EFIR is 19H, the CR19 register can be accessed through EFDR. The bit definitions are as follows:



This register is used for the high speed modem application. While the bit is set to logic 1 it can make the baudrate of UART up to 921.2KBPS (the clock source of UART is 14.769MHz) for high speed transmit/receive.

Bit 7 - bit 2: Reserved.

FASTA (Bit 1):

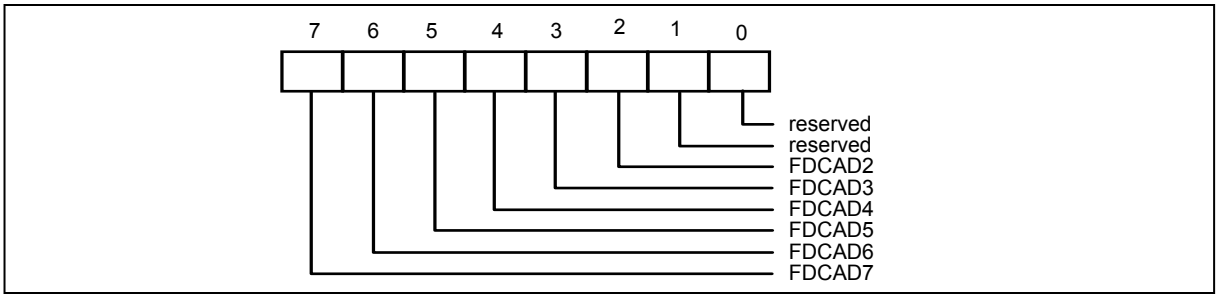
| | |
|---|---|
| 0 | the clock source of UART A is the same as the frequency of TURA (CR0C bit 7) and SUAMIDI (CR3 bit 1) selected. |
| 1 | the clock source of UART A is 14.769MHZ. |

FASTB (Bit 0):

| | |
|---|---|
| 0 | the clock source of UART B is the same as the frequency of TURB (CR0C bit 6) and SUBMIDI (CR3 bit 0) selected. |
| 1 | the clock source of UART B is 14.769MHZ. |

### 11.2.26 Configuration Register 20 (CR20)

When the device is in Extended Function mode and EFIR is 20H, the CR20 register can be accessed through EFDR. Default = FCH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



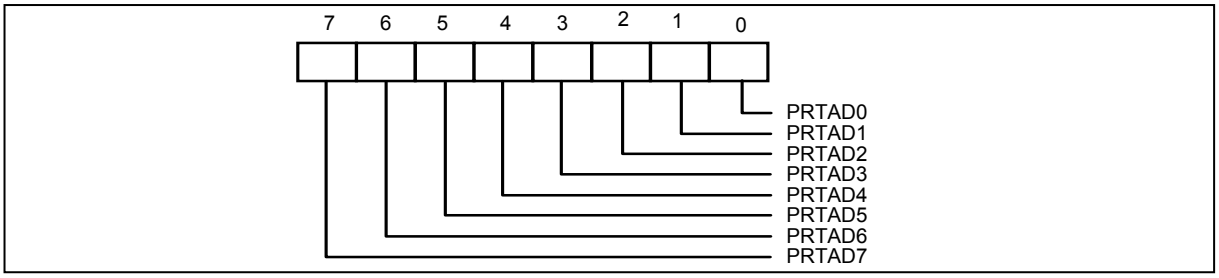

This register is used to select the base address of the Floppy Disk Controller (FDC) from 100H-3F0H on 16-byte boundaries. NCS = 0 and A10 = 0 are required to access the FDC registers. A[3:0] are always decoded as 0xxxb.

FDCAD7-FDCAD2 (Bit 7-bit 2): match A[9:4]. Bit 7 = 0 and bit 6 = 0 disable this decode.

Bit 1-bit 0: Reserved, fixed at zero.

### 11.2.27 Configuration Register 23 (CR23)

When the device is in Extended Function mode and EFIR is 23H, the CR23 register can be accessed through EFDR. Default = DEH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:

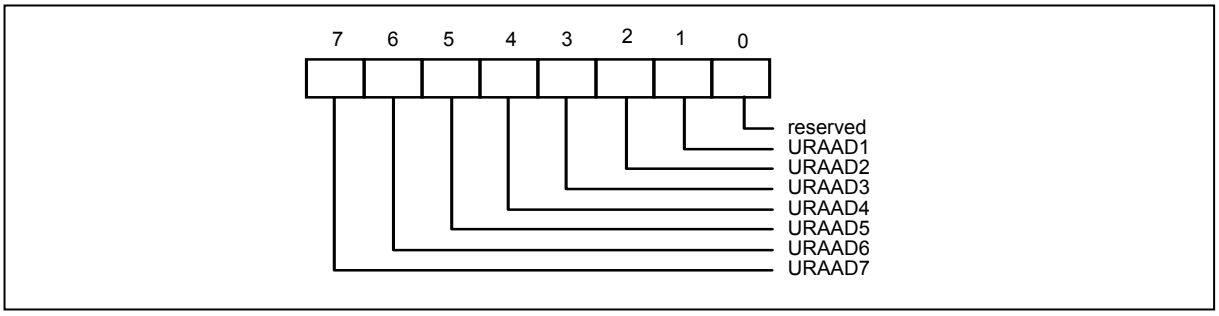



This register is used to select the base address of the parallel port. If EPP is disable, the parallel port can be set from 100H-3FCH on 4-byte boundaries. If EPP is enable, the parallel port can be set from 100H-3F8H on 8-byte boundaries. NCS = 0 and A10 = 0 are required to access the parallel port when in compatible, bi-directional, or EPP modes. A10 is active in ECP mode.

PRTAD7-PRTAD0 (Bit 7-bit 0): match A[9:2]. Bit 7 = 0 and bit 6 = 0 disable this decode.

### 11.2.28 Configuration Register 24 (CR24)

When the device is in Extended Function mode and EFIR is 24H, the CR24 register can be accessed through EFDR. Default = FEH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



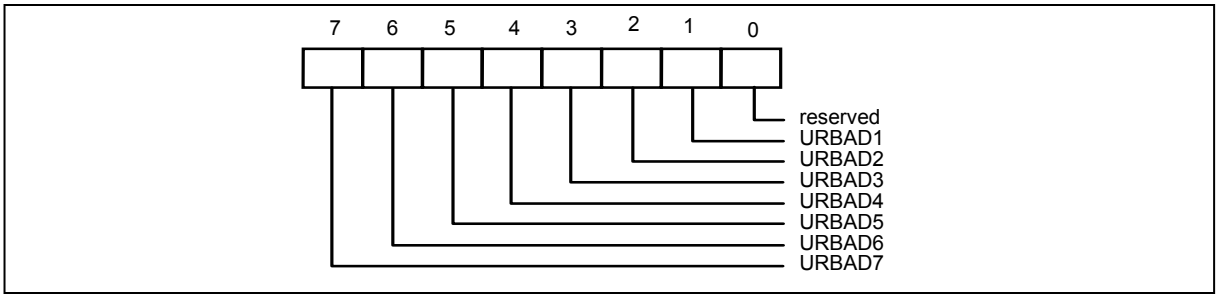

This register is used to select the base address of the UART A from 100H-3F8H on 8-byte boundaries. NCS = 0 and A10 = 0 are required to access the UART A registers. A[2:0] are don't-care conditions.

URAAD7-URAAD1 (Bit 7-bit 1): match A[9:3]. Bit 7 = 0 and bit 6 = 0 disable this decode.

Bit 0: Reserved, fixed at zero.

### 11.2.29 Configuration Register 25 (CR25)

When the device is in Extended Function mode and EFIR is 25H, the CR25 register can be accessed through EFDR. Default = BEH if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



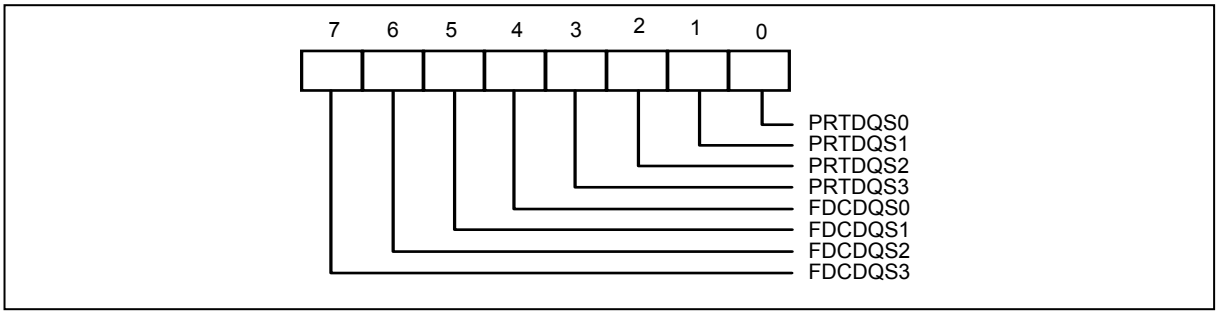
This register is used to select the base address of the UART B from 100H-3F8H on 8-byte boundaries. NCS = 0 and A10 = 0 are required to access the UART B registers. A[2:0] are don't-care conditions.

URBAD7-URBAD1 (Bit 7-bit 1): match A[9:3]. Bit 7 = 0 and bit 6 = 0 disable this decode.

Bit 0: Reserved, fixed at zero.

### 11.2.30 Configuration Register 26 (CR26)

When the device is in Extended Function mode and EFIR is 26H, the CR26 register can be accessed through EFDR. Default = 23H if CR16 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



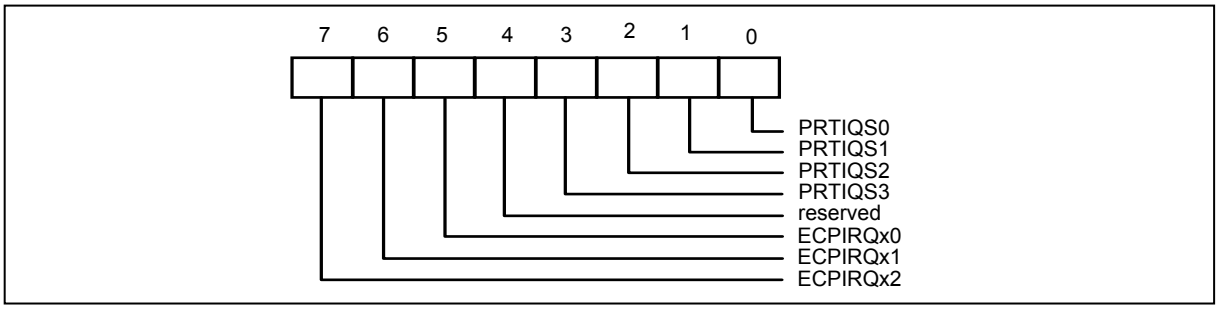

FDCDQS3-FDCDQS0 (Bit 7-bit 4): Allocate DMA resource for FDC.

PRTDQS3-PRTDQS0 (Bit 3-bit 0): Allocate DMA resource for PRT.

| BIT 7- BIT4, BIT 3 - BIT 0 | DMA SELECTED |
|---|---|
| 0000 | None |
| 0001 | DMA_A |
| 0010 | DMA_B |
| 0011 | DMA_C |

### 11.2.31 Configuration Register 27 (CR27)

When the device is in Extended Function mode and EFIR is 27, the CR27 register can be accessed through EFDR. Default = 05H if CR6 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:



ECPIRQx2-ECPIRQx0 (Bit7-bit 5): These bits are configurable equivalents to bit[5:3] of cnfgB register in ECP mode except that cnfgB[5:3] are read-only bits. They indicate the IRQ resource assigned for the ECP printer port. It is the software designer's responsibility to ensure that CR27[7:5] and CR27[3:0] are consistent. For example, CR27[7:5] should be filled with 001 (select IRQ 7) if CR27[3:0] are to be programmed as 0101 (select IRQ_E) while IRQ_E is connected to IRQ 7.

| CR27[7:5] | IRQ RESOURCE |
|---|---|
| 000 | reflect other IRQ resources selected by CR27[3:0] (default) |
| 001 | IRQ 7 |
| 010 | IRQ 9 |
| 011 | IRQ 10 |
| 100 | IRQ 11 |
| 101 | IRQ 14 |
| 110 | IRQ 15 |
| 111 | IRQ 5 |

Bit 4: Reserved.

PRTIQS3-PRTIQS0 (Bit 3-bit 0): Select IRQ resource for the parallel port. Any unselected IRQ pin is in tri-state.

| CR27[3:0] | SELECT IRQ PIN |
|---|---|
| 0000 | None |
| 0001 | IRQ_A |
| 0010 | IRQ_B |
| 0011 | IRQ_C |
| 0100 | IRQ_D |
| 0101 | IRQ_E |
| 0110 | IRQ_F |
| 0111 | IRQ_G |
| 1000 | IRQ_H |

While in the Serial IRQ mode (IRQMODS=1, CR31 bit2), the above selection is invalid and all the IRQ signal pins, from IRQ_A to IRQ_H, are all in tri-state. The parallel port IRQ is dedicated to the SERIRQ pin. For the host controller to correctly sample the parallel port IRQ, the parallel port IRQ should be programmed to appear in one of IRQ/Data Frame sampling periods.

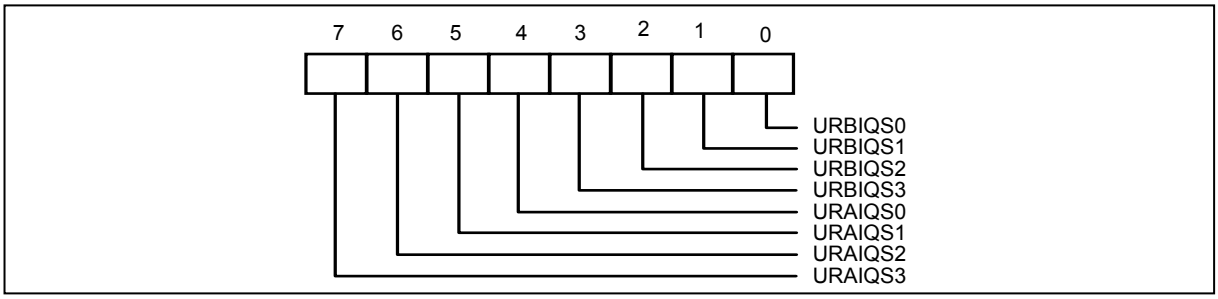
In Serial IRQ mode, the definition of PRTIQS3-PRTIQS0 (bit 3-bit 0) is as follows:

PRTIQS3-PRTIQS0 (Bit 3-bit 0): Select the IRQ/Data Frame sampling period on the SERIRQ pin.

| CR27[3:0] | IRQ/DATA FRAME PERIOD |
|---|---|
| 0000 | None |
| 0001 | IRQ1 |
| 0010 | Reserved for $\overline{SMI}$ |
| 0011 | IRQ3 |
| 0100 | IRQ4 |
| 0101 | IRQ5 |
| 0110 | IRQ6 |
| 0111 | IRQ7 |
| 1000 | IRQ8 |
| 1001 | IRQ9 |
| 1010 | IRQ10 |
| 1011 | IRQ11 |
| 1100 | IRQ12 |
| 1101 | IRQ13 |
| 1110 | IRQ14 |
| 1111 | IRQ15 |

### 11.2.32 Configuration Register 28 (CR28)

When the device is in Extended Function mode and EFIR is 28, the CR28 register can be accessed through EFDR. Default = 43H if CR6 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:

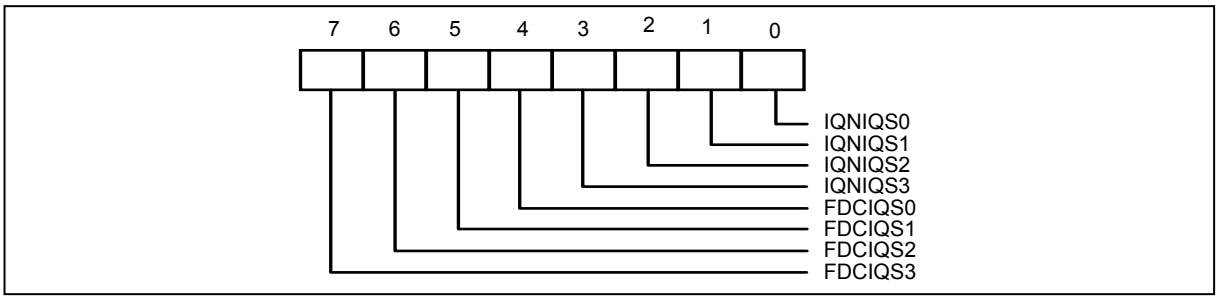



URAIQS3-URAIQS0 (Bit 7-bit 4): Allocate interrupt resource for UART A.

URBIQS3-URBIQS0 (Bit 3-bit 0): Allocate interrupt resource for UART B.

### 11.2.33 Configuration Register 29 (CR29)

When the device is in Extended Function mode and EFIR is 29, the CR29 register can be accessed through EFDR. Default = 62H if CR6 bit 2 = 1; default = 00H if CR16 bit 2 = 0. The bit definitions are as follows:

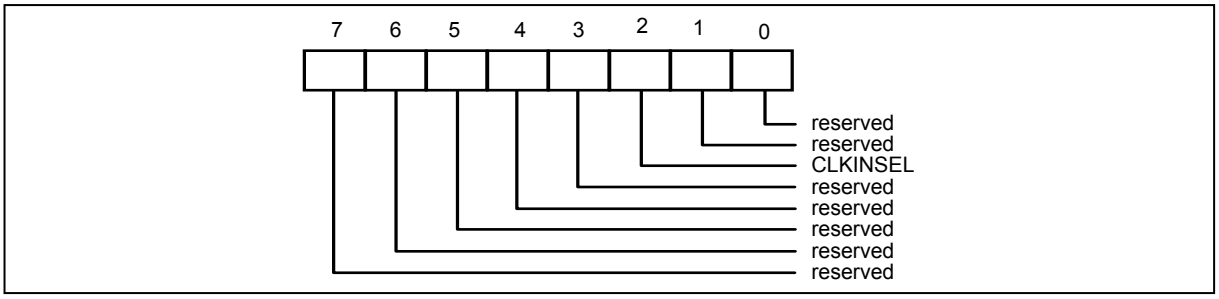



FDCIQS3-FDCIQS0 (Bit 7-bit 4): Allocate interrupt resource for FDC.

IQNIQS3-IQNIQS0 (Bit 3-bit 0): Allocate interrupt resource for IRQIN.

### 11.2.34 Configuration Register 2C (CR2C), default=00H

When the device is in Extended Function mode and EFIR is 2CH, the CR2C register can be accessed through EFDR. The bit definitions are as follows:




Bit 7 - bit 3 : Reserved.

CLKINSEL (Bit 2): Clock input frequency selection.

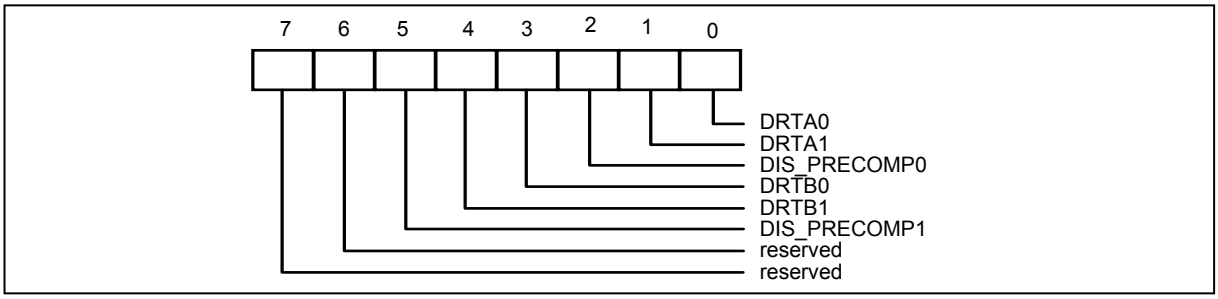
This pin should be reset/set according the CLKIN pin.

| | |
|---|---|
| 0 | the clock source on CLKIN pin is 24 MHz.(default) |
| 1 | the clock source on CLKIN pin is 48 MHz. |

Bit 1- bit 0: Reserved.

### 11.2.35 Configuration Register 2D (CR2D), default=00H

When the device is in Extended Function mode and EFIR is 2DH, the CR2D register can be accessed through EFDR. The bit definitions are as follows:




This register controls the data rate selection for FDC. It also controls if precompensation is enabled.

Bit 7 - bit 6: Reserved.

DIS_PRECOMP1 (Bit 5):

This bit controls if precompensation is enabled for FDD B.

0 enable precompensation for FDD B

1 disable precompensation for FDD B

DRTB1, DRTB0 (Bit 4,3):

These two bits combining with data rate selection bits in Date Rate Register select the operational data rate for FDD B as shown in last table.

DIS_PRECOMP0 (Bit 2):

This bit controls if precompensation is enabled for FDD A.

0 enable precompensation for FDD A

1 disable precompensation for FDD A

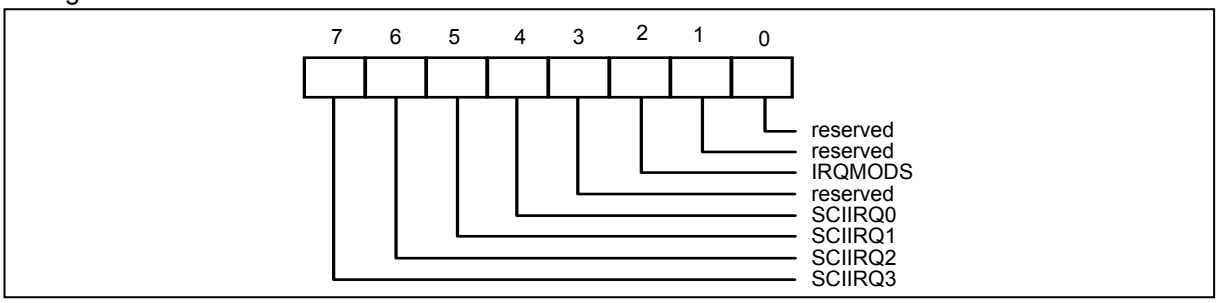
DRTA1, DRTA0 (Bit 1 - bit 0):

These two bits combining with data rate selection bits in Date Rate Register select the operational data rate for FDD A as follows:

| DRIVE RATE TABLE | | DATA RATE | | OPERATIONAL DATA RATE | |
|---|---|---|---|---|---|
| DRTA1 | DRTA0 | DRATE1 | DRATE0 | MFM | FM |
| 0 | 0 | 1 | 1 | 1M | --- |
| 0 | 0 | 0 | 0 | 500K | 250K |
| 0 | 0 | 0 | 1 | 300K | 150K |
| 0 | 0 | 1 | 0 | 250K | 125K |
| 0 | 1 | 1 | 1 | 1M | --- |
| 0 | 1 | 0 | 0 | 500K | 250K |
| 0 | 1 | 0 | 1 | 500K | 250K |
| 0 | 1 | 1 | 0 | 250K | 125K |
| 1 | 0 | 1 | 1 | 1M | --- |
| 1 | 0 | 0 | 0 | 500K | 250K |
| 1 | 0 | 0 | 1 | 2M | --- |
| 1 | 0 | 1 | 0 | 250K | 125K |

### 11.2.36 Configuration Register 31 (CR31), default=00H

When the device is in Extended Function mode and EFIR is 31H, the CR31 register can be accessed through EFDR. The bit definitions are as follows:




SCIIRQ3 ~ SCIIRQ0 (Bit 7 - bit 4):

The four bits select one IRQ pin for the SCI signal except for dedicated SCI signal output pin. Any unselected pin is in tri-state.

| CR31[7:4] | MAPPED IRQ PIN |
|---|---|
| 0000 | None (default) |
| 0001 | IRQ_A |
| 0010 | IRQ_B |
| 0011 | IRQ_C |
| 0100 | IRQ_D |
| 0101 | IRQ_E |
| 0110 | IRQ_F |
| 0111 | IRQ_G |
| 1000 | IRQ_H |

While in the Serial IRQ mode (IRQMODS=1, CR31 bit 2), the above selection is invalid and all the IRQ signal pins, from IRQ_A to IRQ_H, are all in tri-state. The SCI interrupt output is dedicated to the SERIRQ pin. For the host controller to correctly sample the SCI interrupt, the SCI interrupt should be programmed to appear in one of IRQ/Data Frame sampling periods.

In Serial IRQ mode, the definition of SCIIQS3-SCIIQS0 (bit 7-bit 4) is as follows:

SCIIQS3-SCIIQS0 (bit 7-bit 4): Select the IRQ/Data sampling period on the SERIRQ pin.

| CR27[7:4] | IRQ/DATA FRAME PERIOD |
|---|---|
| 0000 | None |
| 0001 | IRQ1 |
| 0010 | Reserved for $\overline{\text{SMI}}$ |
| 0011 | IRQ3 |
| 0100 | IRQ4 |
| 0101 | IRQ5 |
| 0110 | IRQ6 |
| 0111 | IRQ7 |
| 1000 | IRQ8 |
| 1001 | IRQ9 |
| 1010 | IRQ10 |
| 1011 | IRQ11 |
| 1100 | IRQ12 |
| 1101 | IRQ13 |
| 1110 | IRQ14 |
| 1111 | IRQ15 |

Bit 3: Reserved.

IRQMODS (Bit 2):

IRQ mode selection. W83877TF/TG supports: (1) legacy ISA IRQ mode or ISA IRQ sharing mode. (2) Serial IRQ mode used in the PCI bus. In the legacy ISA IRQ sharing mode, the selected IRQ pin for the device's IRQ is defined in the configuration registers CR27 - CR29. In the ISA IRQ sharing mode, configuration register CR18 indicates which IRQ pin is in the IRQ sharing mode.

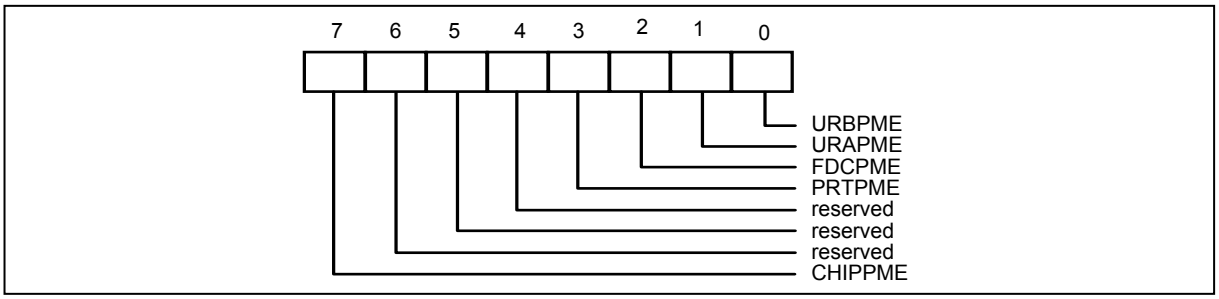
0: legacy ISA IRQ mode or ISA IRQ sharing mode.(default)

1: Serial IRQ mode used in PCI bus.

Bit 1 - bit 0: Reserved.

### 11.2.37 Configuration Register 32 (CR32), default=00H

When the device is in Extended Function mode and EFIR is 32H, the CR32 register can be accessed through EFDR. The bit definitions are as follows:




CHIPPME (Bit 7): W83877TF/TG chip power management enable.

| | |
|---|---|
| 0 | disable the ACPI/Legacy and the auto power management functions. |
| 1 | enable the ACPI/Legacy and the auto power management functions. |

Bit 6 - bit 4: Reserved.

PRTPME (Bit 3): Printer port power management enable.

| | |
|---|---|
| 0 | disable the auto power management function. |
| 1 | enable the auto power management function, if this bit and CHIPPME(CR32 bit 7) are both set to 1. |

.

FDCPME (Bit 2): FDC power management enable.

| | |
|---|---|
| 0 | disable the auto power management function. |
| 1 | enable the auto power management function, if this bit and CHIPPME(CR32 bit 7) are both set to 1. |

.

URAPME (Bit 1): UART A power management enable.

| | |
|---|---|
| 0 | disable and the auto power management function. |
| 1 | enable auto power management function, if this bit and CHIPPME(CR32 bit 7) are both set to 1. |

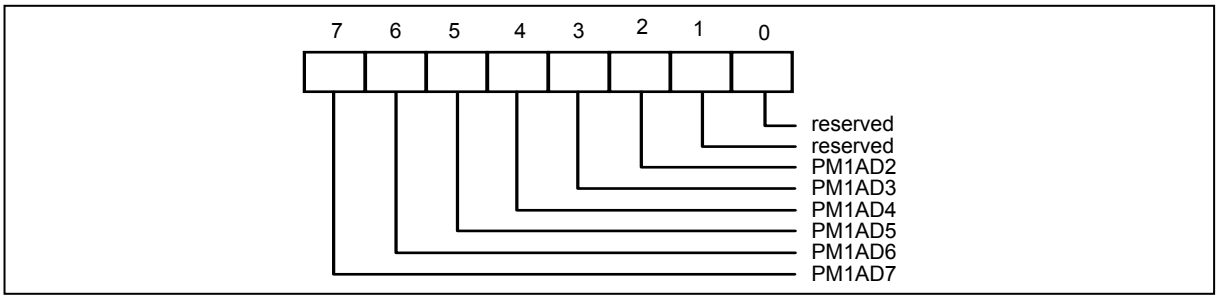
.

URBPME (Bit 0): UART B power management enable.

| | |
|---|---|
| 0 | disable the auto power management functions. |
| 1 | enable the auto power management function, if this bit and CHIPPME(CR32 bit 7) are both set to 1. |

### 11.2.38 Configuration Register 33 (CR33), default=00H

When the device is in Extended Function mode and EFIR is 33H, the CR33 register can be accessed through EFDR. The bit definitions are as follows:



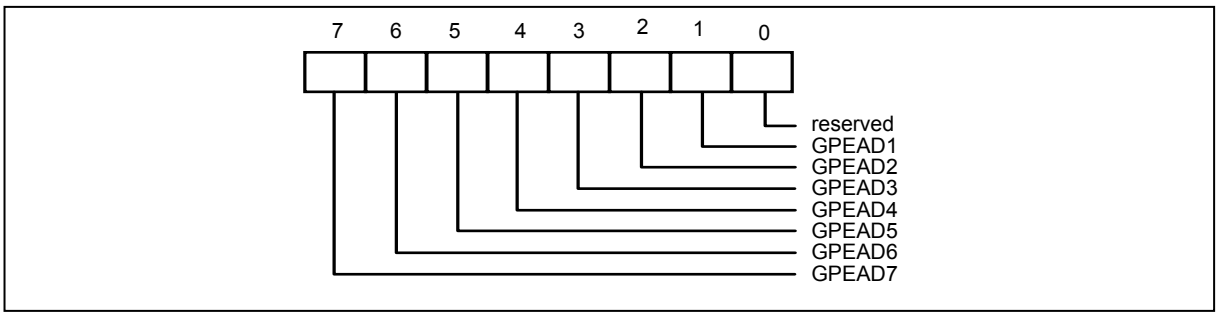

PM1AD7 - PM1AD2 (Bit 7 - bit 2): Base address of the power management register block PM1.

This address is the base address of PM1a_EVT_BLK in the ACPI specification. The based address should range from $01,0000,0000_b$ to $11,1111,0000_b$ ,i.e., 100H ~ 3F0H, where bit 1 and bit 0 of the base address should be set to 0 and the based address is in the 16-byte alignment. Note that the based address of PM1a_CNT_BLK is equal to PM1a_EVT_BLK + 4, and PM_TMR_BLK is equal to PM1a_EVT_BLK + 8.

Bit 1 - bit 0: Reserved, fixed at 0.

### 11.2.39 Configuration Register 34 (CR34), default=00H

When the device is in Extended Function mode and EFIR is 34H, the CR34 register can be accessed through EFDR. The bit definitions are as follows:



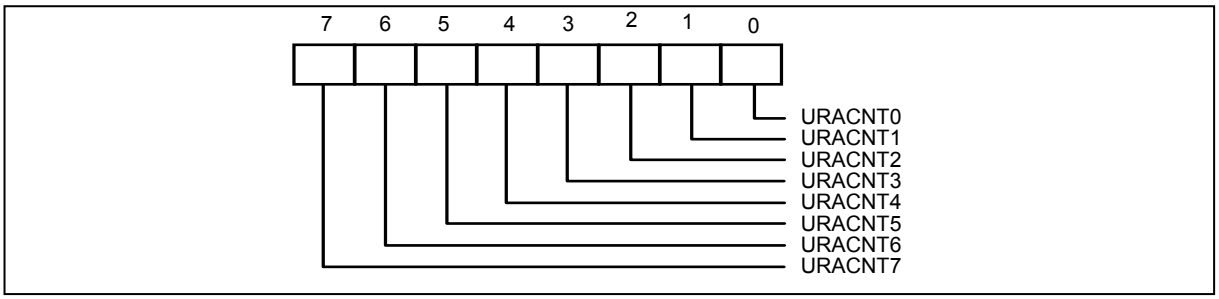
GPEAD7 - GPEAD1 (Bit7 - bit 1): Base address of the power management register block GPE.

This address is the base address of GPE0_BLK in the ACPI specification. The based address should range from $01,0000,0000_b$ to $11,1111,1000_b$ ,i.e., 100H ~ 3F8H, where bit 0 of the base address should be set to 0 and the based address is in the 8-byte alignment. Note that the base address of GPE1_BLK is GPE0_BLK + 4.

Bit 0: Reserved, fixed at 0.

### 11.2.40 Configuration Register 35 (CR35), default=00H

When the device is in Extended Function mode and EFIR is 35H, the CR35 register can be accessed through EFDR. The bit definitions are as follows:

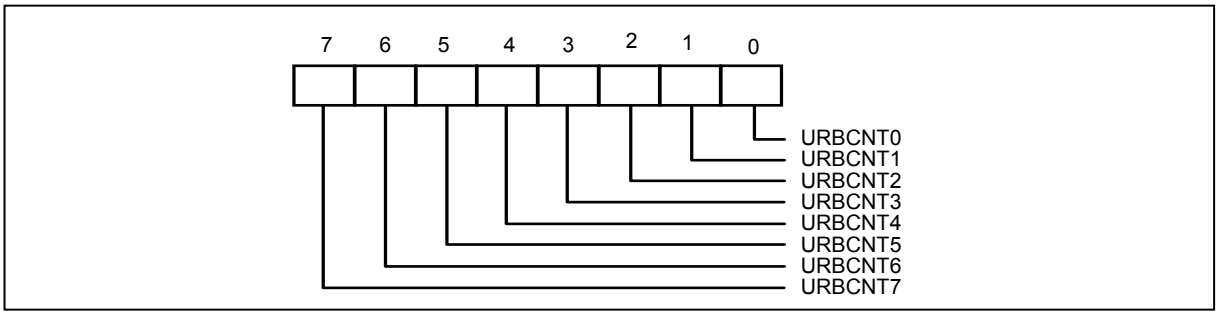



URACNT7 - URACNT0 (Bit 7 - bit 0): UART A idle timer count.

This register is used to specify the initial value of UART A idle timer. Once UART A enters the working state (that is, after any access to this device, any IRQ, and any external input), the power down machine of UART A reloads this count value and the idle timer counts down. When the timer counts down to zero, UART A enters the power down state ,i.e., sleeping state. If this register is set to 00H, the power down function will be invalid. The time resolution of this value is minute or second, which is defined by the TMIN_SEL bit of the CR3A. Note that (1). this register is valid only when the power management function of UART A is enabled, that is, CHIPPME=1 (CR32 bit 7) and URAPME=1 (CR32 bit 1), (2). If the register is set to 00H, UART A will remain in the current state(working or sleeping).

### 11.2.41 Configuration Register 36 (CR36), default=00H

When the device is in Extended Function mode and EFIR is 36H, the CR36 register can be accessed through EFDR. The bit definitions are as follows:

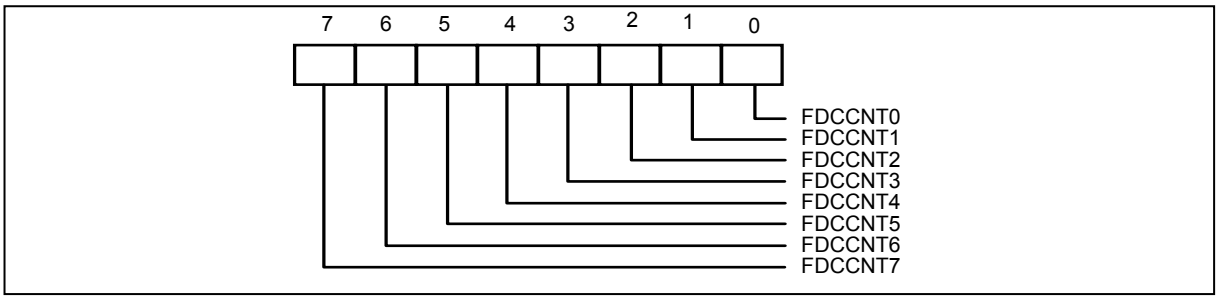


URBCNT7 - URBCNT0 (Bit 7 - bit 0): UART B idle timer count.

This register is used to specify the initial value of UART B idle timer. Once UART B enters the working state (that is, after any access to this device, any IRQ, and any external input), the power down machine of UART B reloads this count value and the idle timer counts down. When the timer counts down to zero, UART B enters the power down state ,i.e., sleeping state. If this register is set to 00H, the power down function will be invalid. The time resolution of this value is minute or second, which is defined by the TMIN_SEL bit of CR3A. Note that (1). this register is valid only when the power management function of UART B is enabled, that is, CHIPPME=1 (CR32 bit 7) and URBPME=1 (CR32 bit 0), (2). If the register is set to 00H, UART B will remain in the current state(working or sleeping).

### 11.2.42 Configuration Register 37 (CR37), default=00H

When the device is in Extended Function mode and EFIR is 37H, the CR37 register can be accessed through EFDR. The bit definitions are as follows:

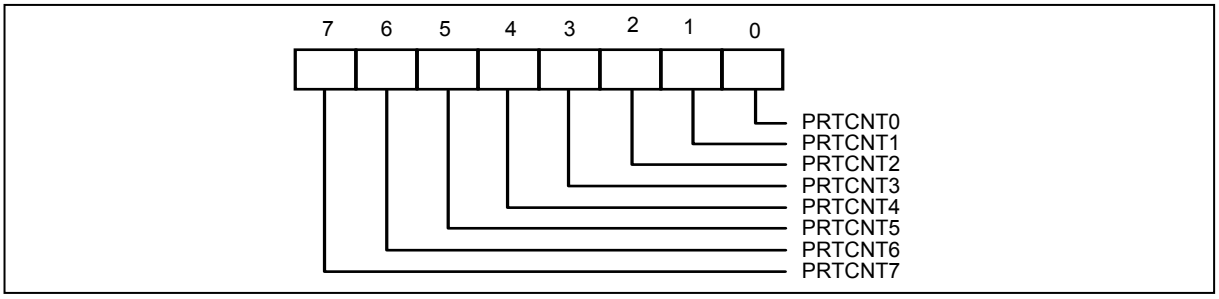



FDCCNT7 - FDCCNT0 (Bit 7 - bit 0): FDC idle timer count.

This register is used to specify the initial value of FDC idle timer. Once FDC enters the working state (that is, after any access to this device, any IRQ, and any external input), the power down machine of FDC reloads this count value and the idle timer counts down. When the timer counts down to zero, FDC enters the power down state ,i.e., sleeping state. If this register is set to 00H, the power down function will be invalid. The time resolution of this value is minute or second, which is defined by the TMIN_SEL bit of the CR3A. Note that (1). this register is valid only when the power management function of FDC is enabled, that is, CHIPPME=1 (CR32 bit 7) and FDCPME=1 (CR32 bit 2), (2). If the register is set to 00H, FDC will remain in the current state(working or sleeping).

### 11.2.43 Configuration Register 38 (CR38), default=00H

When the device is in Extended Function mode and EFIR is 38H, the CR38 register can be accessed through EFDR. The bit definitions are as follows:

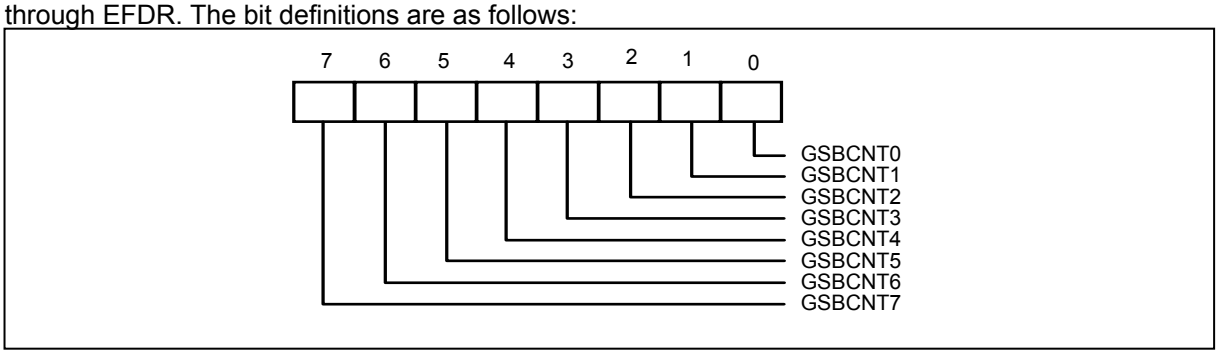


PRTCNT7 - PRTCNT0 (Bit 7 - bit 0): printer port idle timer count.

This register is used to specify the initial value of the printer port idle timer. Once the printer port enters the working state (that is, after any access to this device, any IRQ, and any external input), the power down machine of the printer port reloads this count value and this idle timer counts down. When the timer counts down to zero, printer port enters the power down state ,i.e., sleeping state. If this register is set to 00H, the power down function will be invalid. The time resolution of this value is minute or second, which is defined by the TMIN_SEL bit of CR3A. Note that (1). this register is valid only when the power management function of the printer port is enabled, that is, CHIPPME=1 (CR32 bit 7) and PRTPME=1 (CR32 bit 3), (2). If the register is set to 00H, the printer port will remain in the current state(working or sleeping).

### 11.2.44 Configuration Register (CR39), default=00H

When the device is in Extended Function mode and EFIR is 39H, the CR39 register can be accessed through EFDR. The bit definitions are as follows:

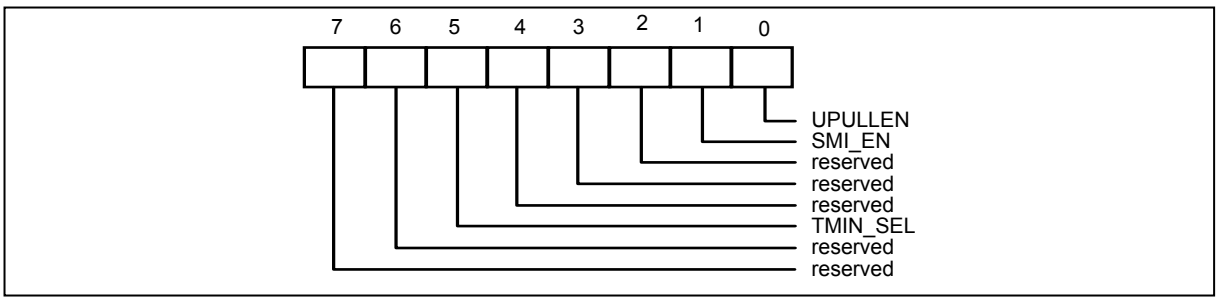



GSBCNT7 - GSBCNT0 (Bit 7 - bit 0): global stand-by idle timer count.

Once all devices of the chip (including UART A, UART B, FDC and the printer port) are in the power down state, the power down machine of W83877TF/TG chip loads this register value and counts down. When the timer counts to zero, the whole chip enters the power down state, i.e., sleeping state. If this register is set to 0, the power down function will be invalid. The time resolution of this register value is minute or second, which is defined by the TMIN_SEL bit of CR3A. Note that (1). this register is valid when the CHIPPME = 1 (CR32 bit 7), and (2) If the register is set to 00H, W83877TF/TG chip will remain in the current state(working or sleeping).

### 11.2.45 Configuration Register 3A (CR3A), default=00H

When the device is in Extended Function mode and EFIR is 3AH, the CR3A register can be accessed through EFDR. The bit definitions are as follows:




Bit 7 - bit 6 : Reserved, fixed at 0.

TMIN_SEL (Bit 5): Time resolution of the auto power machines of all devices.

CR35 to CR39 store the initial counts of the devices.

| | |
|---|---|
| 0 | one second |
| 1 | one minute |

Bit 4 - bit 2: Reserved, fixed at 0.

SMI_EN (Bit 1): SMI output pin enable.

While an SMI event is raised on the output of the SMI logic, this bit determines whether the SMI interrupt will be generated on the SMI output $\overline{\text{SMI}}$ pin and on the Serial IRQ IRQSER pin while in Serial IRQ mode.

| | |
|---|---|
| 0 | disable |
| 1 | enable |

UPULLEN (Bit 0): Enable the pull up of IRQSER pin in Serial IRQ mode.

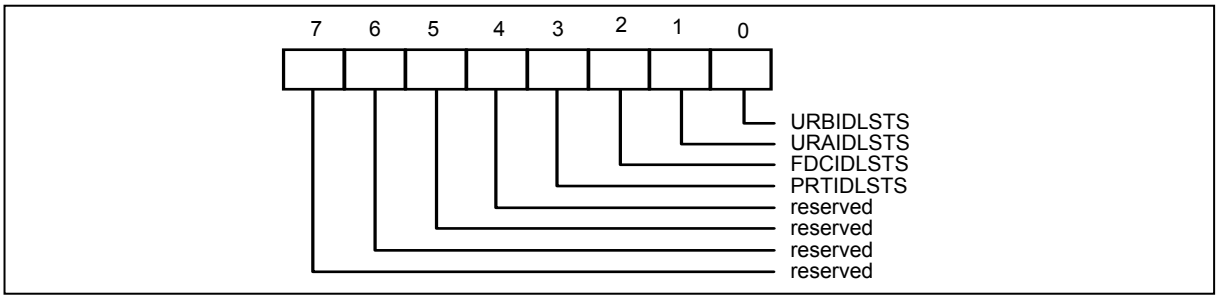
| | |
|---|---|
| 0 | disable the pull up of IRQSER pin. |
| 1 | enable the pull up of IRQSER pin. |

### 11.2.46 Configuration Register 3B (CR3B), default=00H

Reserved for testing. Should be kept all 0's.

### 11.2.47 Configuration Register 40 (CR40), default=00H

When the device is in Extended Function mode and EFIR is 40H, the CR40 register can be accessed through EFDR. The bit definitions are as follows:




Bit 7 - bit 4 : Reserved, fixed at 0.

Bit 3 - bit 0 : Devices' idle status.

These bits indicate that the individual device's idle timer expires due to no I/O access, IRQ, and external input to the device respectively. These 4 bits are controlled by the printer port, FDC, UART A, and UART B power down machines individually. The bits are set/cleared by W83877TF/TG automatically. Writing a 1 can also clear this bit, and writing a 0 has no effect.

PRTIDLSTS (Bit 3): printer port idle status.

| | |
|---|---|
| 0 | printer port is now in the working state. |
| 1 | printer port is now in the sleeping state due to no printer port access, IRQ, DMA acknowledge, and no transition on BUSY, $\overline{ACK}$, PE, SLCT, and $\overline{ERR}$ pins. |

FDCIDLSTS (Bit 2): FDC idle status.

| | |
|---|---|
| 0 | FDC is now in the working state. |
| 1 | FDC is now in the sleeping state due to no FDC access, no IRQ, no DMA acknowledge, and no enabling of the motor enable bits in the DOR register. |

URAIDLSTS (Bit 1): UART A idle status.

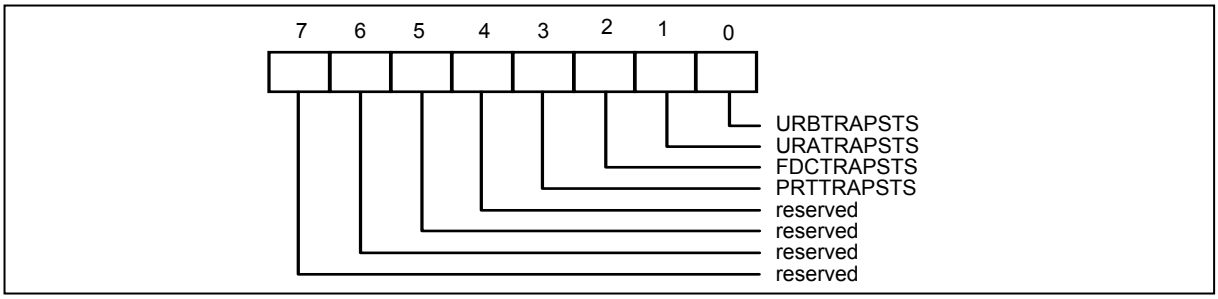
| | |
|---|---|
| 0 | UART A is now in the working state. |
| 1 | UART A is now in the sleeping state due to no UART A access, no IRQ, the receiver is now waiting for a start bit, the transmitter shift register is now empty, and no transition on MODEM control input lines. |

URBIDLSTS (Bit 0): UART B idle status.

| | |
|---|---|
| 0 | UART B is now in the working state. |
| 1 | UART B is now in the sleeping state due to no UART B access, no IRQ, the receiver is now waiting for a start bit, the transmitter shift register is now empty, and no transition on MODEM control input lines. |

### 11.2.48 Configuration Register 41 (CR41), default=00H

When the device is in Extended Function mode and EFIR is 41H, the CR41 register can be accessed through EFDR. The bit definitions are as follows:




Bit 7 - bit 4 : Reserved, fixed at 0.

Bit 3 - bit 0 : Devices' trap status.

These bits indicate that the individual device wakes up due to any I/O access, IRQ, and external input to the device respectively. The device's idle timer reloads the initial count value from CR35-CR39, depending on which device wakes up. These 4 bits are controlled by the printer port, FDC, UART A, and UART B power down machines individually. The bits are set/cleared by W83877TF/TG automatically. Writing a 1 can also clear this bit, and writing a 0 has no effect.

PRTTRAPSTS (Bit 3): printer port trap status.

| | |
|---|---|
| 0 | the printer port is now in the sleeping state. |
| 1 | the printer port is now in the working state due to any printer port access, any IRQ, any DMA acknowledge, and any transition on BUSY, $\overline{ACK}$, PE, SLCT, and $\overline{ERR}$ pins. |

FDCTRAPSTS (Bit 2): FDC trap status.

| | |
|---|---|
| 0 | FDC is now in the sleeping state. |
| 1 | FDC is now in the working state due to any FDC access, any IRQ, any DMA acknowledge, and any enabling of the motor enable bits in the DOR register. |

URATRAPSTS (Bit 1): UART A trap status.

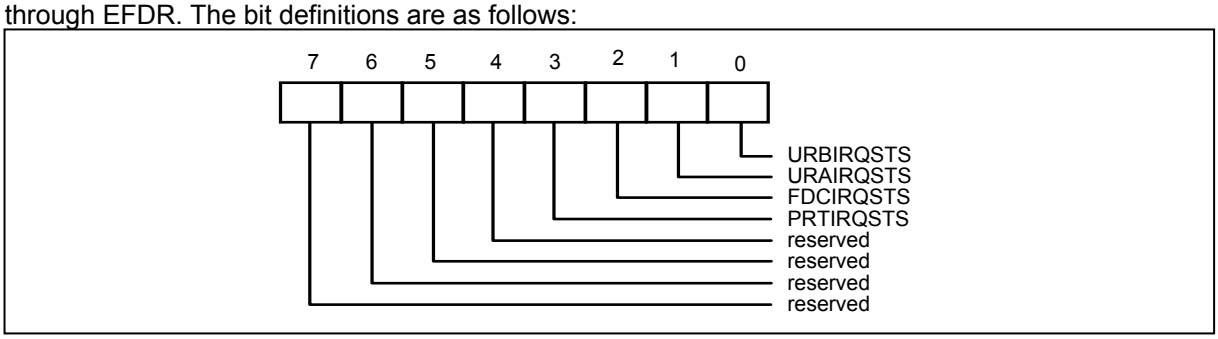
| | |
|---|---|
| 0 | UART A is now in the sleeping state. |
| 1 | UART A is now in the working state due to any UART A access, any IRQ, the receiver begins receiving a start bit, the transmitter shift register begins transmitting a start bit, and any transition on MODEM control input lines. |

URBTRAPSTS (Bit 0): UART B trap status.

| | |
|---|---|
| 0 | UART B is now in the sleeping state. |
| 1 | UART B is now in the working state due to any UART B access, any IRQ, the receiver begins receiving a start bit, the transmitter shift register begins transmitting a start bit, and any transition on MODEM control input lines. |

### 11.2.49 Configuration Register 42 (CR42), default=N/A

When the device is in Extended Function mode and EFIR is 42H, the CR42 register can be accessed through EFDR. The bit definitions are as follows:




Bit 7 - bit 4 : Reserved, fixed at 0.

Bit 3 - bit 0 : Device's IRQ status .

These bits indicate the IRQ pin status of the individual device respectively. The device's IRQ status bit is set or cleared at their source device, writing a 1 or 0 has no effect.

PRTIRQSTS (Bit 3) : printer port IRQ status. While the IRQ type of printer port is edge trigger-type, this bit will set and reset immediately. As the software reads this bit, it indicates low level. The software must read the IRQ status bit in the printer port device register to correctly identify whether the printer port IRQ occurs.

FDCIRQSTS (Bit 2) : FDC IRQ status.

URAIRQSTS (Bit 1) : UART A IRQ status.

URBIRQSTS (Bit 0) : UART B IRQ status.

### 11.2.50 Configuration Register 43 (CR43), default=00H

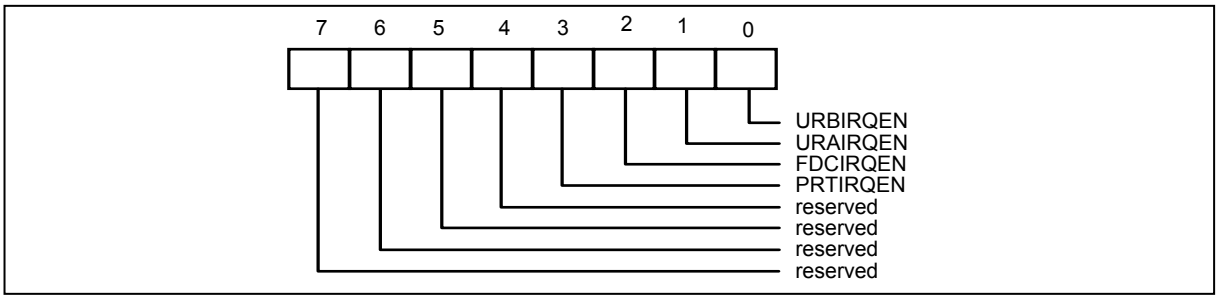
When the device is in Extended Function mode and EFIR is 43H, the CR43 register can be accessed through EFDR. This register is reserved.

### 11.2.51 Configuration Register 44 (CR44), default=00H

When the device is in Extended Function mode and EFIR is 44H, the CR44 register can be accessed through EFDR. This register is reserved.

### 11.2.52 Configuration Register 45 (CR45), default=00H

When the device is in Extended Function mode and EFIR is 45H, the CR45 register can be accessed through EFDR. The bit definitions are as follows:




Bit 7 - bit 4 : Reserved, fixed at 0.

Bit 3 - bit 0 : Enable bits of the SMI generation due to the device's IRQ.

These bits enable the generation of an SMI interrupt due to any IRQ of the devices respectively. These 4 bits control the printer port, FDC, UART A, and UART B SMI logic's individually. The SMI logic output for the IRQs is as follows:

SMI logic output = (URBIRQEN and URBIRQSTS) or (URAIRQEN and URAIRQSTS) or (FDCIRQEN and FDCIRQSTS) or (PRTIRQEN and PRTIRQSTS)

If any device's IRQ is raised, the corresponding IRQ status bit in CR42 is set. If the device's enable bit is set and SMI_EN(in CR3A) and CHIPPME(in CR32) is both set, then SMI interrupt occurs on the SMI output pin.

PRTIRQEN (Bit 3):

| | |
|---|---|
| 0 | disable the generation of an SMI interrupt due to the printer port's IRQ. |
| 1 | enable the generation of an SMI interrupt due to the printer port's IRQ. |

FDCIRQEN (Bit 2):

| | |
|---|---|
| 0 | disable the generation of an SMI interrupt due to the FDC's IRQ. |
| 1 | enable the generation of an SMI interrupt due to the FDC's IRQ. |

URAIRQEN (Bit 1):

| | |
|---|---|
| 0 | disable the generation of an SMI interrupt due to the UART A's IRQ. |
| 1 | enable the generation of an SMI interrupt due to the UART A's IRQ. |

URBIRQEN (Bit 0):

| | |
|---|---|
| 0 | disable the generation of an SMI interrupt due to the UART B's IRQ. |
| 1 | enable the generation of an SMI interrupt due to the UART B's IRQ. |

### 11.2.53 Bit Map Configuration Registers

Table 11-1: Bit Map of Configuration Registers

| Register | Power-on Reset Value | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| CR0 | 0000 0000 | 0 | 0 | 0 | 0 | PRTMODS1 | PRTMODS0 | 0 | IPD |
| CR1 | 0000 0000 | ABCHG | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CR2 | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CR3 | 0011 0000 | 0 | 0 | EPPVER | 0 | 0 | 0 | SUAMIDI | SUBMIDI |
| CR4 | 0000 0000 | PRTPWD | 0 | URAPWD | URBPWD | PRTTRI | 0 | URATRI | URBTRI |
| CR5 | 0000 0000 | 0 | 0 | 0 | 0 | ECPFTHR3 | ECPFTHR2 | ECPFTHR1 | ECPFTHR0 |
| CR6 | 0000 0000 | 0 | 0 | SEL4FDD | FIPURDWN | FDCPWD | 0 | FDCTRI | 0 |
| CR7 | 0000 0000 | FDD D T1 | FDD D T0 | FDD C T1 | FDD C T0 | FDD B T1 | FDD B T0 | FDD A T1 | FDD A T0 |
| CR8 | 0000 0000 | 0 | 0 | DISFDDWR | SWWP | MEDIA 1 | MEDIA 0 | BOOT 1 | BOOT 0 |
| CR9 | 0000 1010 | PRTMODS2 | LOCKREG | EN3MODE | 0 | CHIP ID 3 | CHIP ID 2 | CHIP ID 1 | CHIP ID 0 |
| CRA | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRB | 0000 1100 | 0 | Tx4WC | Rx4WC | ENIFCHG | IDENT | MFM | INVERTZ | DRV2EN |
| CRC | 0010 1000 | TURA | TURB | HEFERE | 0 | URIRSEL | 0 | RX2INV | TX2INV |
| CRD | 1010 0011 | SIRTX1 | SIRTX0 | SIRRX1 | SIRRX0 | HDUPLX | IRMODE2 | IRMODE1 | IRMODE0 |
| CR10 | 0000 0000 | GIO0AD7 | GIO0AD6 | GIO0AD5 | GIO0AD4 | GIO0AD3 | GIO0AD2 | GIO0AD1 | GIO0AD0 |
| CR11 | 0000 0000 | G0CADM1 | G0CADM0 | 0 | 0 | 0 | GIO0AD10 | GIO0AD9 | GIO0AD8 |
| CR12 | 0000 0000 | GIO1AD7 | GIO1AD6 | GIO1AD5 | GIO1AD4 | GIO1AD3 | GIO1AD2 | GIO1AD1 | GIO1AD0 |
| CR13 | 0000 0000 | G1CADM1 | G1CADM0 | 0 | 0 | 0 | GIO1AD10 | GIO1AD9 | GIO1AD8 |
| CR14 | 0000 0000 | GIOP0MD2 | GIOP0MD1 | GIOP0MD0 | GIO0CSH | GCS0IOR | GCS0IOW | GDA0OPI | GDA0IPI |
| CR15 | 0000 0000 | GIOP1MD2 | GIOP1MD1 | GIOP1MD0 | GIO1CSH | GCS1IOR | GCS1IOW | GDA1OPI | GDA1IPI |
| CR16 | 00ss 0s0s[1] | 0 | 0 | G1IQSEL | G0IQSEL | 0 | PNPCVS | 0 | HEFRAS |
| CR17 | 0000 0000 | 0 | 0 | 0 | PRIRQOD | DSFDLGRQ | DSPRLGRQ | DSUALGRQ | DSUBLGRQ |
| CR18 | 0000 0000 | SHARH | SHARG | SHARF | SHARE | SHARD | SHARC | SHARB | SHARA |
| CR19 | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | FASTA | FASTB |
| CR20 | 1111 1100[2] | FDCAD7 | FDCAD6 | FDCAD5 | FDCAD4 | FDCAD3 | FDCAD2 | 0 | 0 |
| CR23 | 1101 1110[2] | PRTAD7 | PRTAD6 | PRTAD5 | PRTAD4 | PRTAD3 | PRTAD2 | PRTAD1 | PRTAD0 |
| CR24 | 1111 1110[2] | URAAD7 | URAAD6 | URAAD5 | URAAD4 | URAAD3 | URAAD2 | URAAD1 | 0 |
| CR25 | 1011 1110[2] | URBAD7 | URBAD6 | URBAD5 | URBAD4 | URBAD3 | URBAD2 | URBAD1 | 0 |
| CR26 | 0010 0011[2] | FDCDQS3 | FDCDQS2 | FDCDQS1 | FDCDQS0 | PRTDQS3 | PRTDQS2 | PRTDQS1 | PRTDQS0 |

Bit Map Configuration Registers, continued

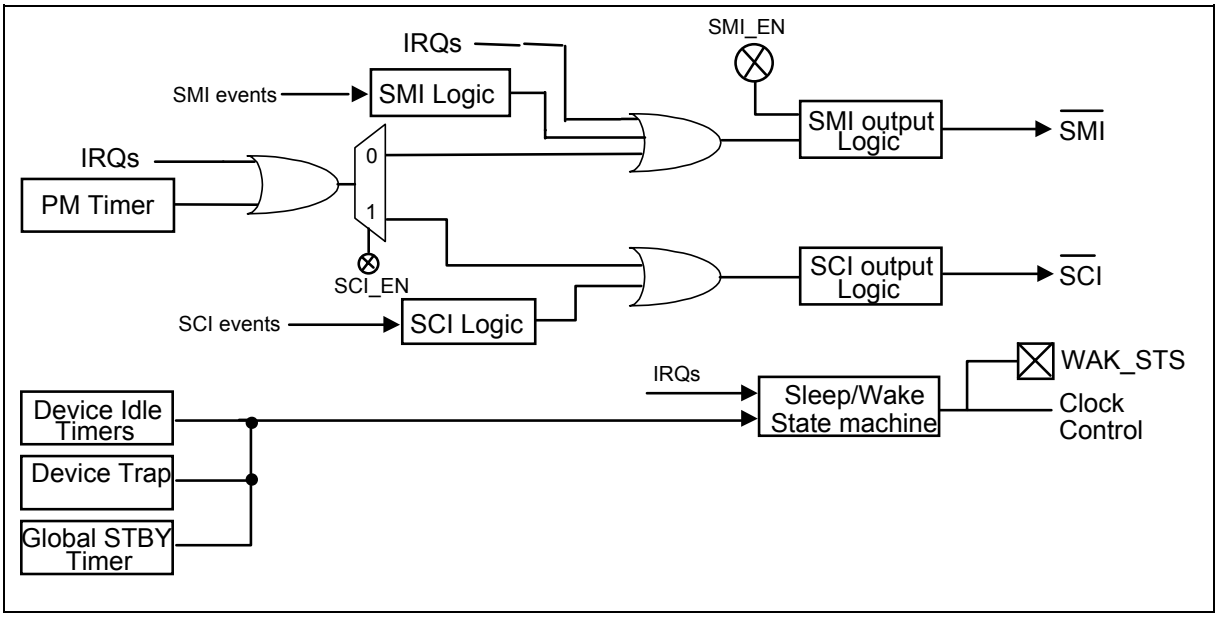
| Register | Power-on Reset Value | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| CR27 | 0000 0101$_2$ | ECPIRQx2 | ECPIRQx1 | ECPIRQx0 | 0 | PRTIQS3 | PRTIQS2 | PRTIQS1 | PRTIQS0 |
| CR28 | 0100 0011$_2$ | URAIQS3 | URAIQS2 | URAIQS1 | URAIQS0 | URBIQS3 | URBIQS2 | URBIQS1 | URBIQS0 |
| CR29 | 0110 0000$_2$ | FDCIQS3 | FDCIQS2 | FDCIQS1 | FDCIQS0 | IQNIQS3 | IQNIQS2 | IQNIQS1 | IQNIQS0 |
| CR2C | 0000 0000 | 0 | 0 | 0 | 0 | 0 | CLKINSEL | 0 | 0 |
| CR2D | 0000 0000 | 0 | 0 | DIS-PRECOM1 | DRTB 1 | DRTB 0 | DIS-PRECOM0 | DRTA 1 | DRTA 0 |
| CR31 | 0000 0s00 | SCIIRQ3 | SCIIRQ2 | SCIIRQ1 | SCIIRQ0 | 0 | IRQMODS | 0 | 0 |
| CR32 | 0000 0000 | CHIPPME | 0 | 0 | 0 | PRTPME | FDCPME | URAPME | URBPME |
| CR33 | 0000 0000 | PM1AD7 | PM1AD6 | PM1AD5 | PM1AD4 | PM1AD3 | PM1AD2 | 0 | 0 |
| CR34 | 0000 0000 | GPEAD7 | GPEAD6 | GPEAD5 | GPEAD4 | GPEAD3 | GPEAD2 | GPEAD1 | 0 |
| CR35 | 0000 0000 | URACNT7 | URACNT6 | URACNT5 | URACNT4 | URACNT3 | URACNT2 | URACNT1 | URACNT0 |
| CR36 | 0000 0000 | URBCNT7 | URBCNT6 | URBCNT5 | URBCNT4 | URBCNT3 | URBCNT2 | URBCNT1 | URBCNT0 |
| CR37 | 0000 0000 | FDCCNT7 | FDCCNT6 | FDCCNT5 | FDCCNT4 | FDCCNT3 | FDCCNT2 | FDCCNT1 | FDCCNT0 |
| CR38 | 0000 0000 | PRTCNT7 | PRTCNT6 | PRTCNT5 | PRTCNT4 | PRTCNT3 | PRTCNT2 | PRTCNT1 | PRTCNT0 |
| CR39 | 0000 0000 | GSBCNT7 | GSBCNT6 | GSBCNT5 | GSBCNT4 | GSBCNT3 | GSBCNT2 | GSBCNT1 | GSBCNT0 |
| CR3A | 0000 0000 | 0 | 0 | TMIN_SEL | 0 | 0 | 0 | SMI_EN | UPULLEN |
| CR40 | 0000 0000 | 0 | 0 | 0 | 0 | PRTIDLSTS | FDCIDLSTS | URAIDLSTS | URBIDLSTS |
| CR41 | 0000 0000 | 0 | 0 | 0 | 0 | PRTTRAPSTS | FDCTRAPSTS | URATRAPSTS | URBTRAPSTS |
| CR42 | 0000 0000 | 0 | 0 | 0 | 0 | PRTIRQSTS | FDCIRQSTS | URAIRQSTS | URBIRQSTS |
| CR43 | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CR44 | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CR45 | 0000 0000 | 0 | 0 | 0 | 0 | PRTIRQEN | FDCIRQEN | URAIRQEN | URBIRQEN |

**Notes:**

1. 's' means its value depends on corresponding power-on setting pin.
2. These default values are valid when CR16 bit 2 is 1 during power-on reset; They will be all 0's if CR16 bit 2 is 0.

## 11.3 ACPI Registers Features

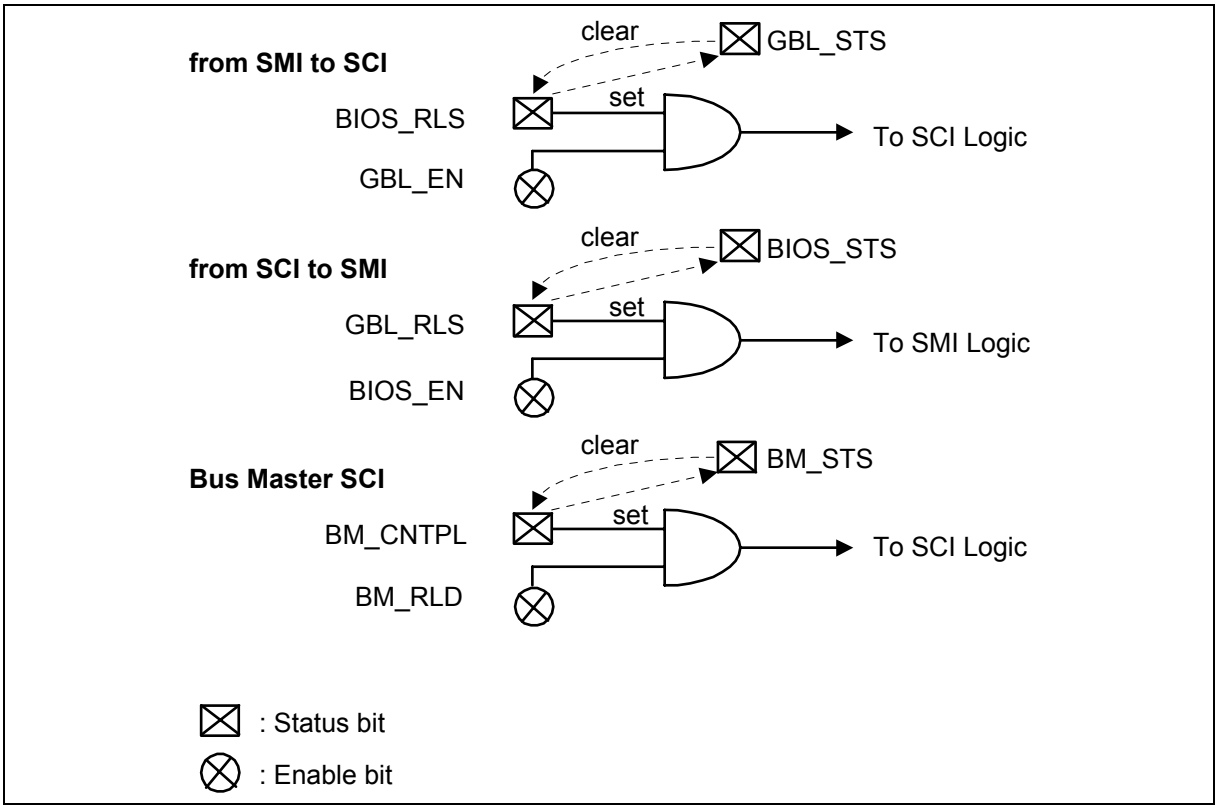
W83877TF/TG supports both the ACPI and legacy power management's. The switch logic of the power management block generates an SMI interrupt in the legacy mode and an SCI interrupt in the ACPI mode. For the legacy mode, the SMI_EN bit is used. If it is set, it routes the power management events from the SMI interrupt logic to the SMI output pin. For the ACPI mode, the SCI_EN bit is used. If it is set, it route the power management events to the SCI interrupt logic. The SMI_EN bit is located in the CR3A register and the SCI_EN bit is located in the PM1 register block. See the following figure for illustration.




The SMI interrupt is routed to pin $\overline{SMI}$, which is dedicated for the SMI interrupt output. Another way to output the SMI interrupt is to route to pin IRQSER, which is the signal pin in the Serial IRQ mode. The SCI interrupt is routed to pin $\overline{SCI}$, which is dedicated for the SCI function. The other way to output the SCI interrupt is to route to one interrupt request signal pin IRQA~H, which is selected through CR31 bit[7:4]. Another way is output the SCI interrupt is to route to pin IRQSER.

SMI to SCI/SCI to SMI and Bus Master

For the process of generating an interrupt from SMI to SCI or from SCI to SMI, see the following figure for illustration.



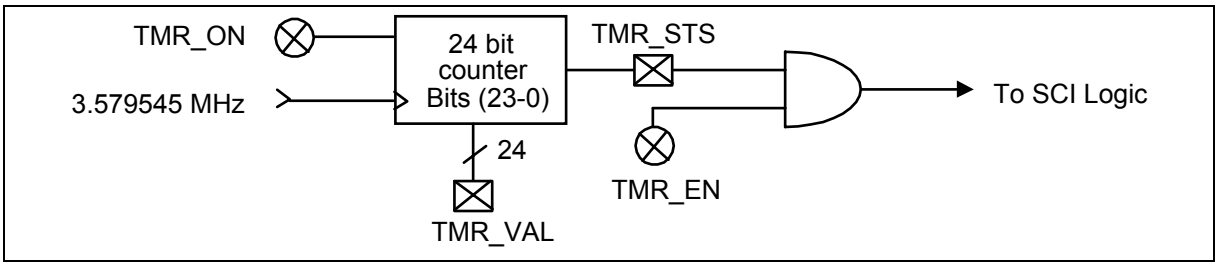

For the BIOS software to raise an event to the ACPI software, BIOS_RLS, GBL_EN, and GBL_STS bits are involved. GBL_EN is the enable bit and the GBL_STS is the status bit. Both are controlled by the ACPI software. If BIOS_RLS is set by the BIOS software and GBL_EN is set by the ACPI software, an SCI interrupt is raised. Writing a 1 to BIOS_RLS sets it to logic 1 and also sets GBL_STS to logic 1; Writing a 0 to BIOS_RLS has no effect. Writing a 1 to GBL_STS clears it to logic 0 and also clears BIOS_RLS to logic 0; writing a 0 to GBL_STS has no effect.

For the ACPI software to raise an event to the BIOS software, GBL_RLS, BIOS_EN, and BIOS_STS bits are involved. BIOS_EN is the enable bit and the BIOS_STS is the status bit. Both are controlled by the BIOS software. If GBL_RLS is set by the ACPI software and BIOS_EN is set by the BIOS software, an SMI is raised. Writing a 1 to GBL_RLS sets it to logic 1 and also sets BIOS_STS to logic 1; Writing a 0 to GBL_RLS has no effect. Writing a 1 to BIOS_STS clears it to logic 0 and also clears GBL_RLS to logic 0; writing a 0 to BIOS_STS has no effect.

For the bus master to raise an event to the ACPI software, BM_CNTRL, BM_RLD, and BM_STS bits are involved. Both BM_RLD and BM_STS are controlled by the ACPI software. If BM_CNTRL is set by the BIOS software and BM_RLD is set by the ACPI software, an SCI interrupt is raised. Writing a 1 to BM_CNTRL sets it to logic 1 and also sets BM_STS to logic 1; Writing a 0 to BM_CNTRL has no effect. Writing a 1 to BM_STS clears it to logic 0 and also clears BM_CNTRL to logic 0; writing a 0 to BM_STS has no effect.

Power Management Timer

In the ACPI specification, it requires a power management timer. The power management timer is a 24-bit fixed rate free running count-up timer that runs off a 3.579545MHZ clock. The power management timer has the corresponding status bit (TMR_STS) and enable bit (TMR_EN). The TMR_STS bit is set any time the last bit of the timer (bit 23) goes from 0 to 1 or from 1 to 0. If the TMR_EN bit is set, the setting of the TMR_STS bit will generate an SCI interrupt. Three registers are used to read the timer value, they are located in the PM1 register block. The power management timer has one enable bit (TMR_ON) to turn if on or off. The TMR_ON is located in GPE register block. If it is cleared to 0, the power management timer function would not work. There are no timer reset requirements, except that the timer should function after power-up. See the following figure for illustration.




## 11.4 ACPI Registers (ACPIRs)

The ACPI register model consists of the fixed register blocks that perform the ACPI functions. A register block may be a event register block which deals with ACPI events or a control register block which deals with control features. The ordering in the event register block is the status register, followed by the enable register.

Each event register, if implemented, contains two two register: a status register and an enable register, both in 16-bit size. The status register indicates what defined function needs the ACPI System Control Interrupt (SCI). While the hardware event occurs, the defined status bit is set. However, to generate the SCI, the associated enable bit is required to be set. If the enable bit is not set, the software can examine the state of the hardware event by reading the status bit without generating an SCI interrupt.

Any status bit, unless otherwise noted, can only be set by some defined hardware event. It is cleared by writing a 1 to its bit position and writing a 0 has no effect. Except for some special status bits, every status bit has an associated enable bit in the same bit position in the enable register. Those status bits which have no respective enable bit are read for special purposes. Revered or un-implemented enable bits always return zero, and writing to these bits should have no effect.

The control bit in the control register provides some special control functions over the hardware event, or some special control over SCI event. Reversed or un-implemented control bits always return zero, and writing to those bits should have no effect.

Table 11-4 lists the PM1 register block and the relative locations of the registers within it. The base address of PM1 register block is named as PM1a_EVT_BLK in the ACPI specification. The based address should range from $01,0000,0000_b$ to $11,1111,0000_b$ ,i.e., 100H ~ 3F0H, where bit 1 and bit 0 of PM1 register block should be set to 0 and the based address is in the 16-byte alignment.

Table 11-5 lists the GPE register block and the relative locations within it. The base address of power management event block GPE is named as GPE0_BLK in the ACPI specification. The based address should range from $01,0000,0000_b$ to $11,1111,1000_b$ ,i.e., 100H ~ 3F8H, where bit 0 of the base address should be set to 0 and the base address is in the 8-byte alignment.

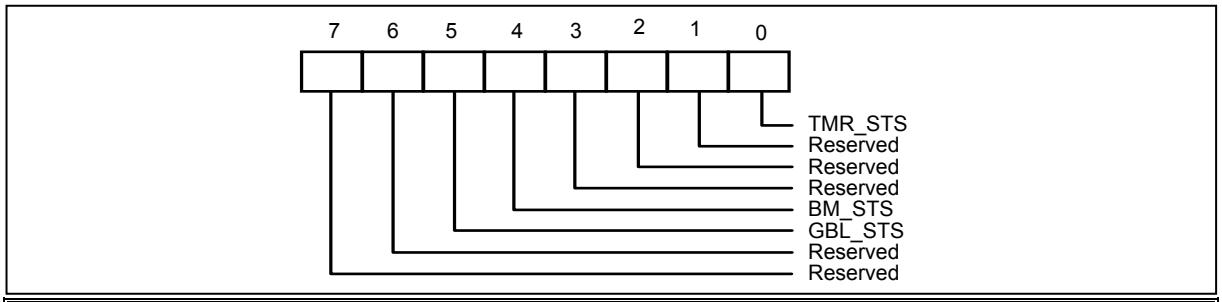
### 11.4.1 Power Management 1 Status Register 1 (PM1STS1)

Register Location: <CR33> System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | TMR_STS | This bit is the timer carry status bit. This bit gets set anytime the bit 23 of the 24-bit counter changes(whenever the MSB changes from low to high or high to low). While TMR_EN and TMR_STS are set a power magnet event is raised. This bit is only set by hardware and can only be cleared by the software writing a 1 to this bit position. Writing a 0 has no effect. |
| 1-3 | Reserved | Reserved. |
| 4 | BM_STS | This is the bus master status bit. Writing a 1 to BM_CNTRL also sets BM_STS. Writing a 1 clears this bit and also clears BM_CNTRL. Writing a 0 has no effect. |
| 5 | GBL_STS | This is the global status bit. This bit is set when the BIOS want the attention of the SCI handler. BIOS sets this bit by setting BIOS_RLS and can only be cleared by software writing a 1 to this bit position. Writing a 1 to this bit position also clears BIOS_RLS. Writing a 0 has no effect. |
| 6-7 | Reserved | Reserved. These bits always return a value of zero. |

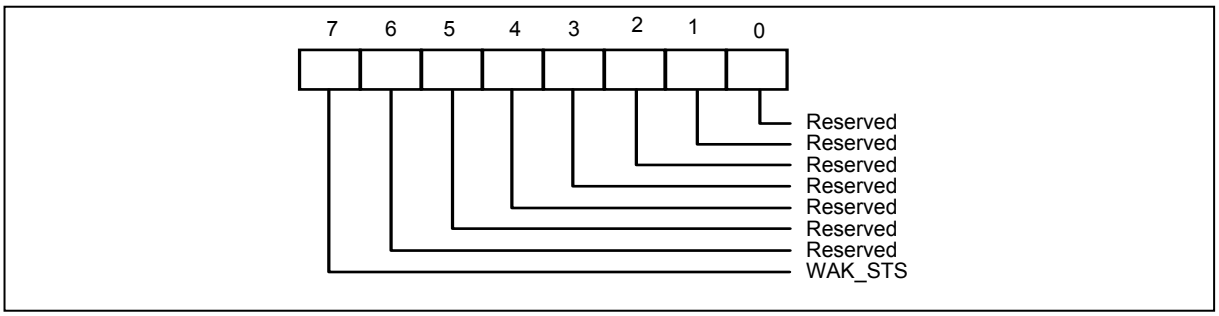
### 11.4.2 Power Management 1 Status Register 2 (PM1STS2)

Register Location: <CR33>+1H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits



| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0-6 | Reserved | Reserved. |
| 7 | WAK_STS | This bit is set when the system is in the sleeping state and an enabled resume event occurs. Upon setting this bit, the sleeping/working state machine will transition the system to the working state. This bit is only set by hardware and is cleared by software writing a 1 to this bit position or by the sleeping/working state machine automatically upon the global standby timer expires. Writing a 0 has no effect. Once the WAK_STS is cleared and all devices have been in sleeping state, the whole chip enters the sleeping state. |

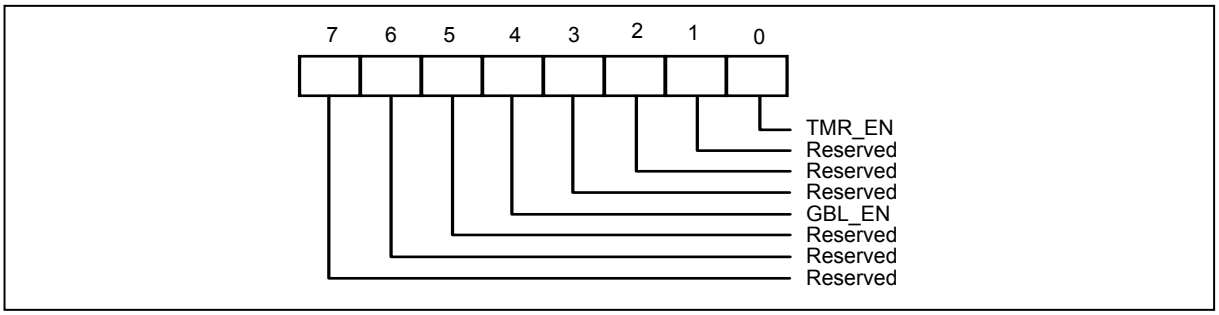
### 11.4.3 Power Management 1 Enable Register 1(PM1EN1)

Register Location: <CR33>+2H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | TMR_EN | This is the timer carry interrupt enable bit. When this bit is set then an SCI event is generated anytime the TMR_STS bit is set. When this bit is reset then no interrupt is generated when the TMR_STS bit is set. |
| 1-4 | Reserved | Reserved. These bits always return a value of zero. |
| 5 | GBL_EN | The global enable bit. When both the GBL_EN bit and the GBL_STS bit are set, an SCI interrupt is raised. |
| 6-7 | Reserved | Reserved. |

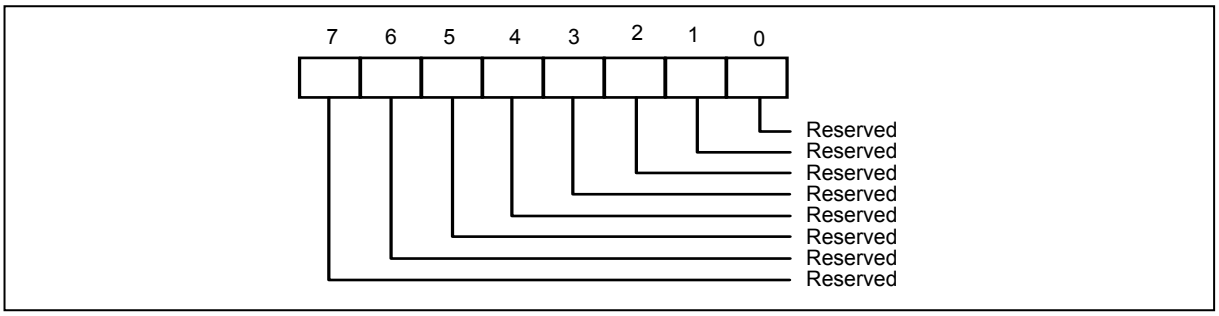
### 11.4.4 Power Management 1 Enable Register 2 (PM1EN2)

Register Location: <CR33>+3H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0-7 | Reserved | Reserved. These bits always return a value of zero. |

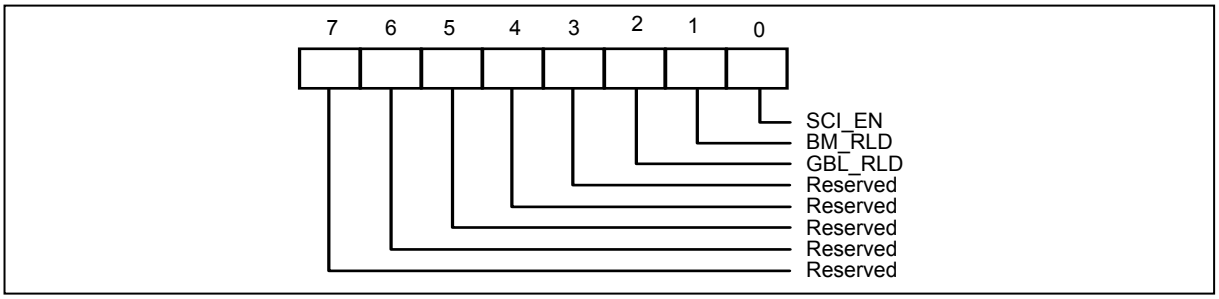
### 11.4.5 Power Management 1 Control Register 1 (PM1CTL1)

Register Location: <CR33>+4H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | SCI_EN | Selects the power management event to be either an SCI or an SMI interrupt. When this bit is set, then the power management events will generate an SCI interrupt. When this bit is reset and SMI_EN bit is set, then the power management events will generate an SMI interrupt. |
| 1 | BM_RLD | This is the bus master reload enable bit. If this bit is set and BM_CNTRL is set, an SCI interrupt is raised. |
| 2 | GBL_RLS | The global release bit. This bit is used by the ACPI software to raise an event to the BIOS software. The BIOS software has a corresponding enable and status bit to control its ability to receive the ACPI event. Setting GBL_RLS sets BIOS_STS, and it generates an SMI interrupt if BIOS_EN is also set. |
| 3-7 | Reserved | Reserved. These bits always return a value of zero. |

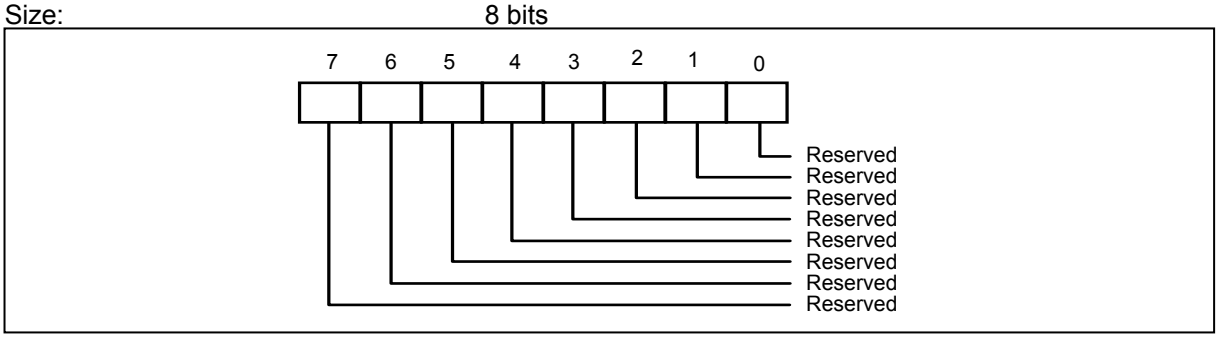
### 11.4.6 Power Management 1 Control Register 2 (PM1CTL2)

Register Location: <CR33>+5H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0-7 | Reserved | Reserved. These bits always return a value of zero. |

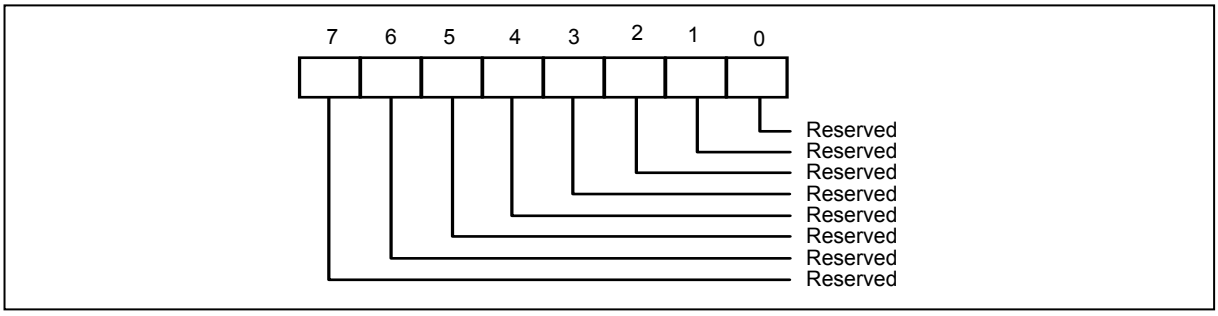
### 11.4.7 Power Management 1 Control Register 3 (PM1CTL3)

Register Location: <CR33>+6H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0-7 | Reserved | Reserved. These bits always return a value of zero. |

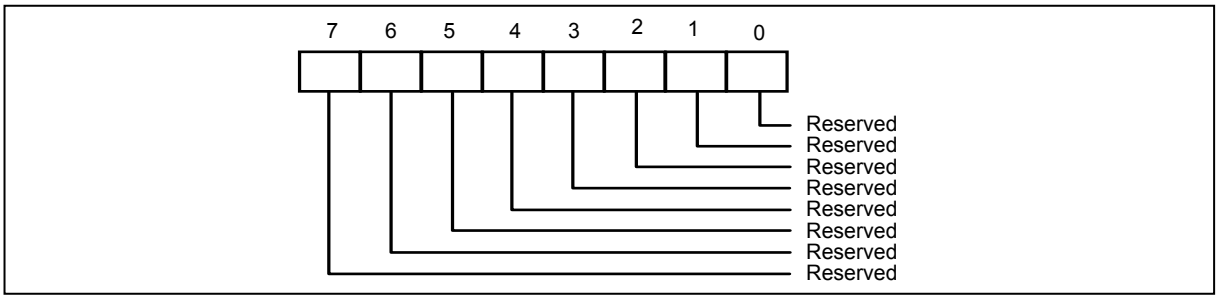
### 11.4.8 Power Management 1 Control Register 4 (PM1CTL4)

Register Location: <CR33>+7H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0-7 | Reserved | Reserved. These bits always return a value of zero. |

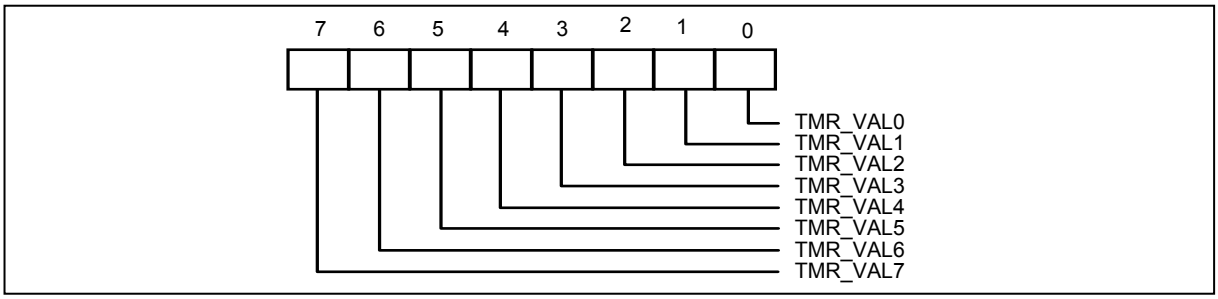
### 11.4.9 Power Management 1 Timer 1 (PM1TMR1)

Register Location: <CR33>+8H System I/O Space

Default Value: 00h

Attribute: Read only

Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0-7 | TMR_VAL | This read-only field returns the running count of the power management timer. This is a 24-bit counter that runs off of a 3.579545 MHZ clock, and counts while in the system working state. The timer is reset and then continues counting until the CLKIN input the the chip is stopped. If the clock is restarted without a MR reset, then the counter will continue counting from where it stopped. The TMR_STS bit is set any time the last bit of the timer (bit 23) goes from 0 to 1 or from 1 to 0. If the TMR_EN bit is set, the setting of the TMR_STS bit will generate an SCI interrupt. |

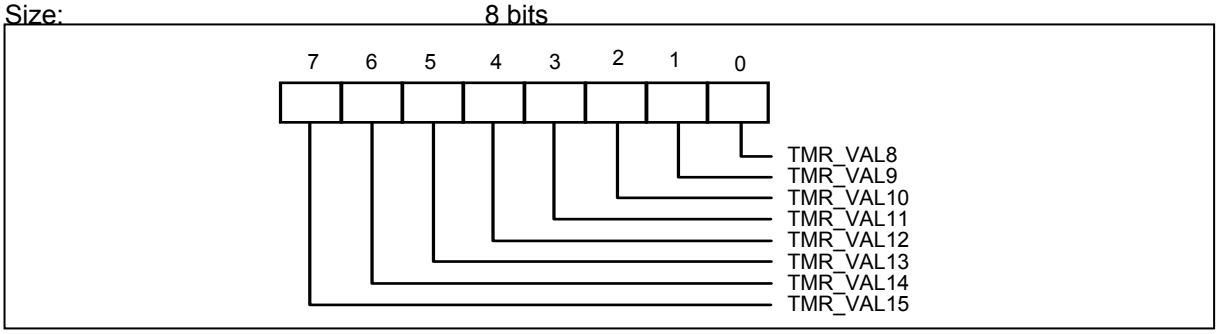
### 11.4.10 Power Management 1 Timer 2 (PM1TMR2)

Register Location: <CR33>+9H System I/O Space

Default Value: 00h

Attribute: Read only

Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0-7 | TMR_VAL | This read-only field returns the running count of the power management timer. This is a 24-bit counter that runs off of a 3.579545 MHZ clock, and counts while in the system working state. The timer is reset and then continues counting until the CLKIN input the the chip is stopped. If the clock is restarted without a MR reset, then the counter will continue counting from where it stopped. The TMR_STS bit is set any time the last bit of the timer (bit 23) goes from 0 to 1 or from 1 to 0. If the TMR_EN bit is set, the setting of the TMR_STS bit will generate an SCI interrupt. |

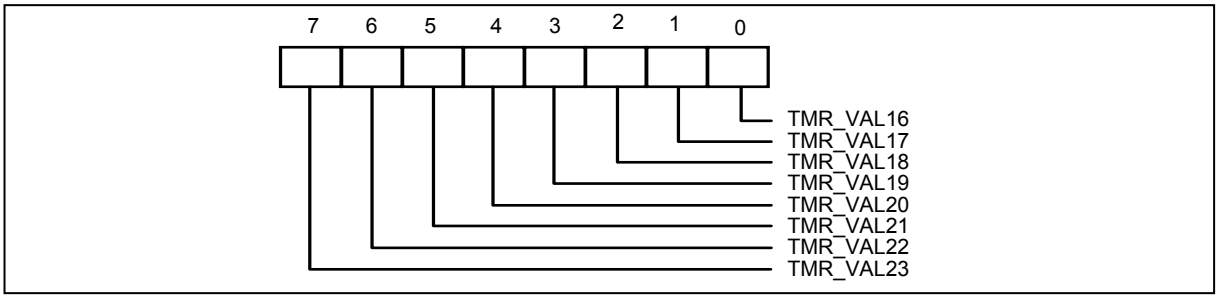
### 11.4.11 Power Management 1 Timer 3 (PM1TMR3)

Register Location: <CR33>+AH System I/O Space

Default Value: 00h

Attribute: Read only

Size: 8 bits



| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0-7 | TMR_VAL | This read-only field returns the running count of the power management timer. This is a 24-bit counter that runs off of a 3.579545 MHZ clock, and counts while in the system working state. The timer is reset and then continues counting until the CLKIN input the the chip is stopped. If the clock is restarted without a MR reset, then the counter will continue counting from where it stopped. The TMR_STS bit is set any time the last bit of the timer (bit 23) goes from 0 to 1 or from 1 to 0. If the TMR_EN bit is set, the setting of the TMR_STS bit will generate an SCI interrupt. |

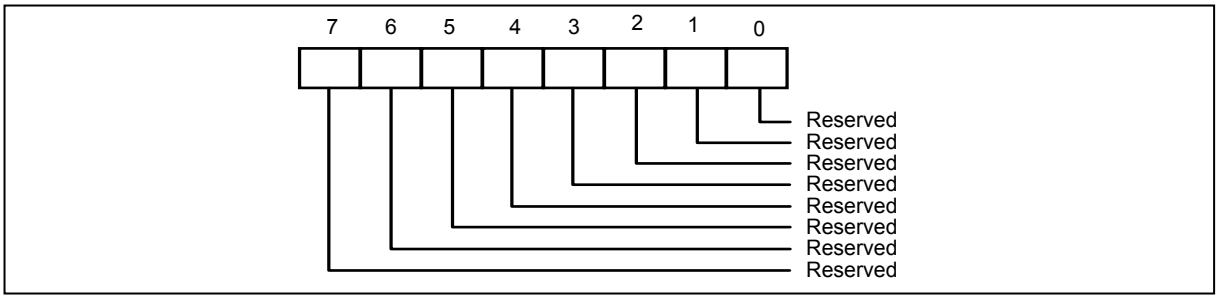
### 11.4.12 Power Management 1 Timer 4 (PM1TMR4)

Register Location: <CR33>+BH System I/O Space

Default Value: 00h

Attribute: Read only

Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0-7 | Reserved | Reserved. These bits always return a value of zero. |

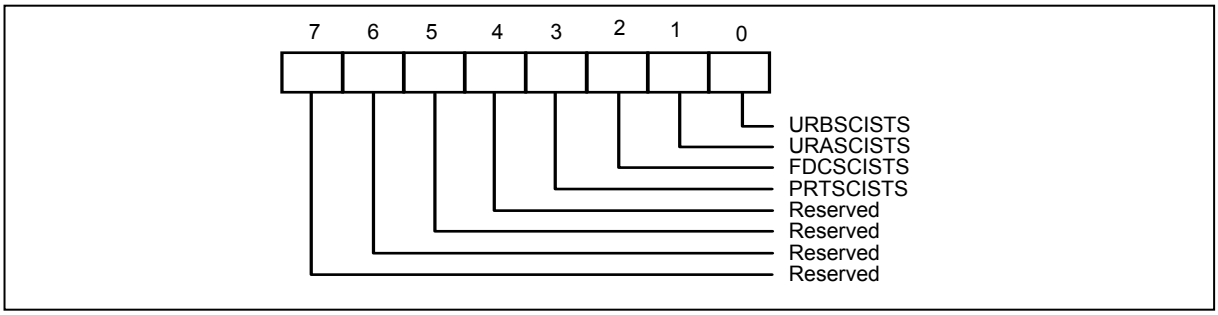
### 11.4.13 General Purpose Event 0 Status Register 1 (GP0STS1)

Register Location: <CR34> System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits



These bits indicate the status of the SCI input, which is set when the device's IRQ is raised. If the corresponding enable bit in the SCI interrupt enable register (in GP0EN1) is set, an SCI interrupt is raised and routed to the output pin. Writing a 1 clears the bit, and writing a 0 has no effect. If the bit is not cleared, new IRQ for the SCI logic input is ignored, therefore no SCI interrupt is raised.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | URBSCISTS | UART B SCI status, which is set by the UART B IRQ. |
| 1 | URASCISTS | UART A SCI status, which is set by the UART A IRQ. |
| 2 | FDCSCISTS | FDC SCI status, which is set by the FDC IRQ. |
| 3 | PRTSCISTS | PRT SCI status, which is set by the printer port IRQ. |
| 4-7 | Reserved | Reserved. |

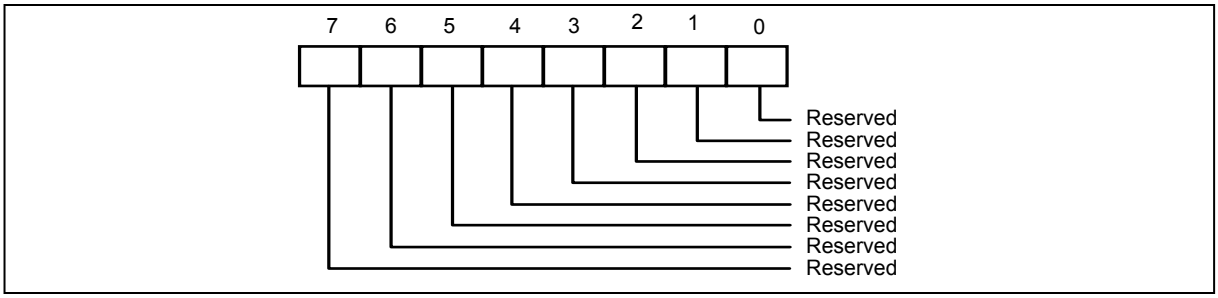
### 11.4.14 General Purpose Event 0 Status Register 2 (GP0STS2)

Register Location: <CR34>+1H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0-7 | Reserved | Reserved. These bits always return a value of zero. |

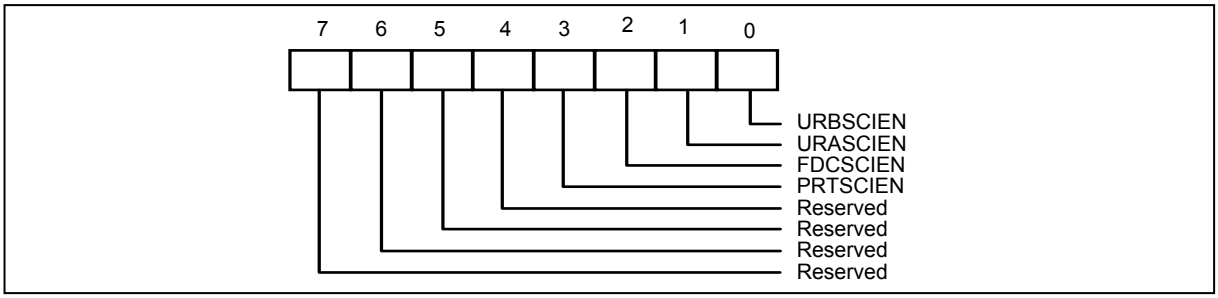
### 11.4.15 General Purpose Event 0 Enable Register 1 (GP0EN1)

Register Location: <CR34> +2H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits




These bits are used to enable the device's IRQ sources onto the SCI logic. The SCI logic output for the IRQs is as follows:

SCI logic output = (URBSCIEN and URBSCISTS) or (URASCIEN and URASCISTS) or (FDCSCIEN and FDCSCISTS) or (PRTSCIEN and PRTSCISTS)

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | URBSCIEN | UART B SCI enable, which controls the UART B IRQ for SCI. |
| 1 | URASCIEN | UART A SCI enable, which controls the UART A IRQ for SCI. |
| 2 | FDCSCIEN | FDC SCI enable, which controls the FDC IRQ for SCI. |
| 3 | PRTSCIEN | printer port SCI enable, which controls the printer port IRQ for SCI. |
| 4-7 | Reserved | Reserved. |

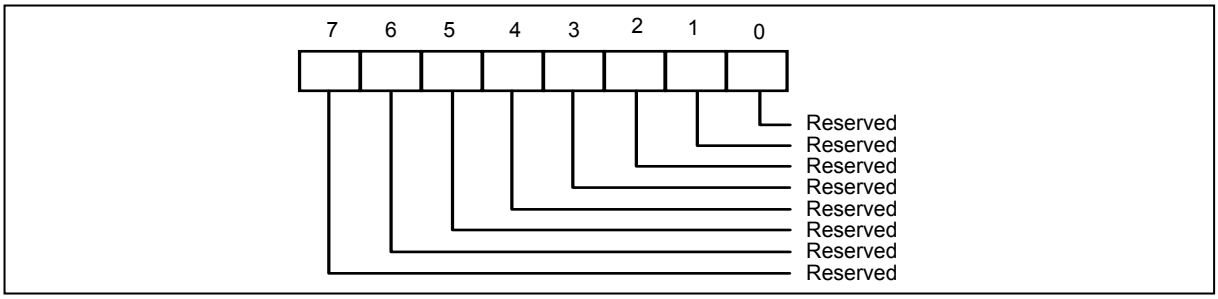
### 11.4.16 General Purpose Event 0 Enable Register 2 (GP0EN2)

Register Location: <CR34>+3H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0-7 | Reserved | Reserved. These bits always return a value of zero. |

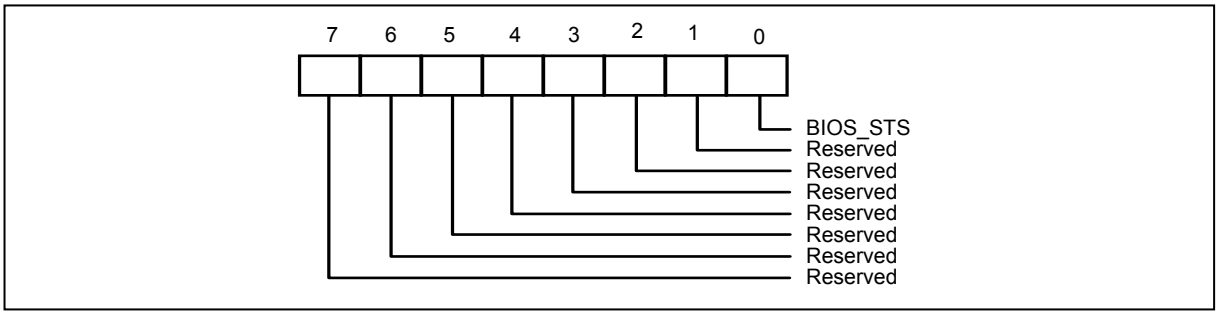
### 11.4.17 General Purpose Event 1 Status Register 1 (GP1STS1)

Register Location: <CR34>+4H System I/O Space

Default Value: 00h

Attribute: Read/write

Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | BIOS_STS | The BIOS status bit. This bit is set when GBL_RLS is set. If BIOS_EN is set, setting GBL_RLS will raise an SMI event. Writing a 1 to its bit location clears BIOS_STS and also clears GBL_RLS. Writing a 0 has no effect. |
| 1-7 | Reserved | Reserved. |

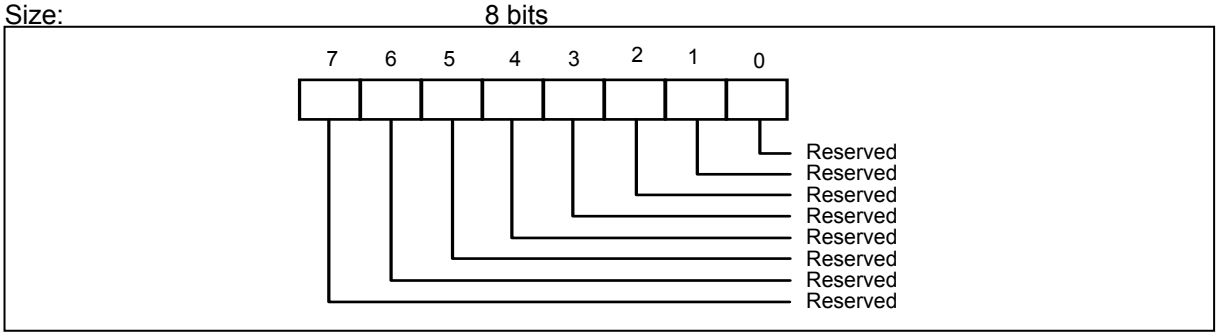
### 11.4.18 General Purpose Event 1 Status Register 2 (GP1STS2)

Register Location: <CR34>+5H System I/O Space

Default Value: 00h

Attribute: Read/write

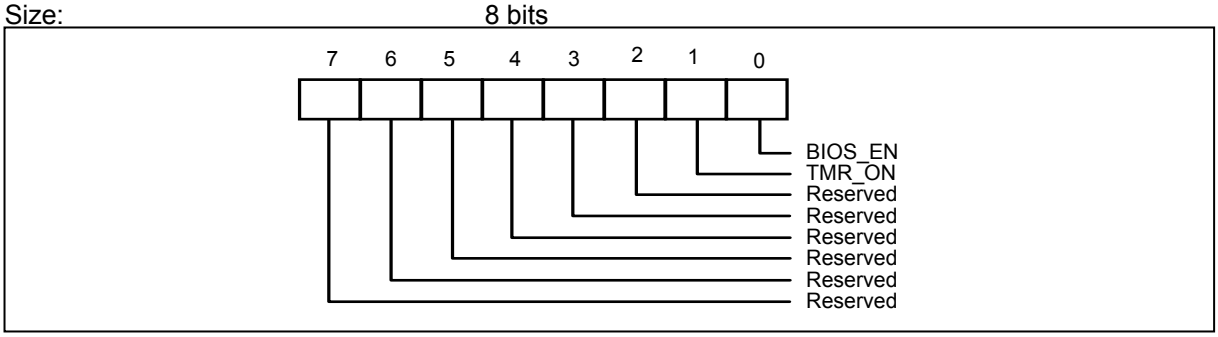
Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0-7 | Reserved | Reserved. These bits always return a value of zero. |

### 11.4.19 General Purpose Event 1 Enable Register 1 (GP1EN1)

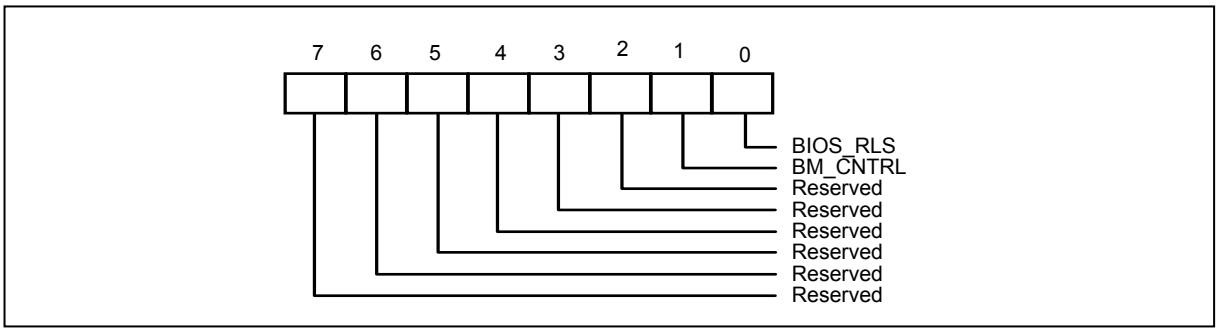
Register Location: <CR34>+6H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits




| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | BIOS_EN | This bit is raise the SMI event. When this bit is set and the ACPI software writes a 1 to the GBL_RLS bit, an SMI event is raised on the SMI logic output. |
| 1 | TMR_ON | This bit is used to turn on the power management timer. 1: timer on ; 0: timer off. |
| 2-7 | Reserved | Reserved. |

### 11.4.20 General Purpose Event 1 Enable Register 2 (GP1EN2)

Register Location: <CR34>+7H System I/O Space
Default Value: 00h
Attribute: Read/write
Size: 8 bits



| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | BIOS_RLS | The BIOS release bit. This bit is used by the BIOS software to raise an event to the ACPI software. The ACPI software has a corresponding enable and status bit to control its ability to receive the ACPI event. Setting BIOS_RLS sets GBL_STS, and it generates an SCI interrupt if GBL_EN is also set. Writing a 1 to its bit position sets this bit and also sets the BM_STS bit. Writing a 0 has no effect. This bit is cleared by writing a 1 to the GBL_STS bit. |
| 1 | BM_CNTRL | This bit is used to set the BM_STS bit and if the BM_RLD bit is also set, then an SCI interrupt is generated. Writing a 1 sets BM_CNTRL to 1 and also sets BM_STS. Writing a 0 has no effect. Writing a 1 to BM_STS clears BM_STS and also clears BM_CNTRL. |
| 2-7 | Reserved | Reserved. |

### 11.4.21 Bit Map Configuration Registers

Table 11-4: Bit Map of PM1 Register Block

| Register | Address | Power-On Reset Value | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| PM1STS1 | <CR33> | 0000 0000 | 0 | 0 | GBL_STS | BM_STS | 0 | 0 | 0 | TMR_STS |
| PM1STS2 | <CR33>+1H | 0000 0000 | WAK_STS | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PM1EN1 | <CR33>+2H | 0000 0000 | 0 | 0 | GBL_EN | 0 | 0 | 0 | 0 | TMR_EN |
| PM1EN2 | <CR33>+3H | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PM1CTL1 | <CR33>+4H | 0000 0000 | 0 | 0 | 0 | 0 | 0 | GBL_RLS | BM_RLD | SCI_EN |
| PM1CTL2 | <CR33>+5H | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PM1CTL3 | <CR33>+6H | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PM1CTL4 | <CR33>+7H | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PM1TMR1 | <CR33>+8H | 0000 0000 | TMR_VAL7 | TMR_VAL6 | TMR_VAL5 | TMR_VAL4 | TMR_VAL3 | TMR_VAL2 | TMR_VAL1 | TMR_VAL0 |
| PM1TMR2 | <CR33>+9H | 0000 0000 | TMR_VAL15 | TMR_VAL14 | TMR_VAL13 | TMR_VAL12 | TMR_VAL11 | TMR_VAL10 | TMR_VAL9 | TMR_VAL8 |
| PM1TMR3 | <CR33>+AH | 0000 0000 | TMR_VAL23 | TMR_VAL22 | TMR_VAL21 | TMR_VAL20 | TMR_VAL19 | TMR_VAL18 | TMR_VAL17 | TMR_VAL16 |
| PM1TMR4 | <CR33>+BH | 0000 0000 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 |

Table 11-5: Bit Map of GPE Register Block

| Register | Address | Power-On Reset Value | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| GP0STS1 | <CR34> | 0000 0000 | 0 | 0 | 0 | 0 | PRTSCISTS | FDCSCISTS | URASCISTS | URBSCISTS |
| GP0STS2 | <CR34>+1H | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GP0EN1 | <CR34>+2H | 0000 0000 | 0 | 0 | 0 | 0 | PRTSCIEN | FDCSCIEN | URASCIEN | URBSCIEN |
| GP0EN2 | <CR34>+3H | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GP1STS1 | <CR34>+4H | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BIOS_STS |
| GP1STS2 | <CR34>+5H | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GP1EN1 | <CR34>+6H | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | TMR_ON | BIOS_EN |
| GP1EN2 | <CR34>+7H | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | BM_CNTRL | BIOS_RLS |

# 12. SPECIFICATIONS

## 12.1 Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|---|---|---|
| Power Supply Voltage | -0.5 to 7.0 | V |
| Input Voltage | -0.5 to $V_{DD}$+0.5 | V |
| Operating Temperature | 0 to +70 | ° C |
| Storage Temperature | -55 to +150 | ° C |

**Note:** Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

## 12.2 DC CHARACTERISTICS

(Ta = 0° C to 70° C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V)

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNI | CONDITIONS |
|---|---|---|---|---|---|---|
| **$I/O_{8tc}$ - TTL level output pin with source-sink capabilities of 8 mA; CMOS level input voltage** | | | | | | |
| Input Low Voltage | $V_{IL}$ | -0.5 | | 0.3xV | V | |
| Input High Voltage | $V_{IH}$ | 0.7x$V_D$ | | $V_{DD}$+0 | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 8 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -8 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = $V_{DD}$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0V |
| **$I/O_{12t}$ - TTL level bi-directional pin with source-sink capabilities of 12 mA** | | | | | | |
| Input Low Voltage | $V_{IL}$ | -0.5 | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{DD}$+0 | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -12 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = $V_{DD}$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0V |
| **$I/O_{24t}$ - TTL level bi-directional pin with source-sink capabilities of 24 mA** | | | | | | |
| Input Low Voltage | $V_{IL}$ | -0.5 | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{DD}$+0 | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 24 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -24 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = $V_{DD}$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0V |

DC Characteristics, continued

| PARAMETER | SY | MIN. | TYP | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| **$OUT_{8t}$ - TTL level output pin with source-sink capabilities of 8 mA** | | | | | | |
| Output Low Voltage | VOL | | | 0.4 | V | IOL = 8 mA |
| Output High Voltage | VOH | 2.4 | | | V | IOH = -8 mA |
| **$OUT_{12t}$ - TTL level output pin with source-sink capabilities of 12 mA** | | | | | | |
| Output Low Voltage | VOL | | | 0.4 | V | IOL = 12 mA |
| Output High Voltage | VOH | 2.4 | | | V | IOH = -12 mA |
| **$OD_{12}$ - Open-drain output pin with sink capabilities of 12 mA** | | | | | | |
| Output Low Voltage | VOL | | | 0.4 | V | IOL = 12 mA |
| **$OD_{24}$ - Open-drain output pin with sink capabilities of 24 mA** | | | | | | |
| Output Low Voltage | VOL | | | 0.4 | V | IOL = 24 mA |
| **$IN_t$ - TTL level input pin** | | | | | | |
| Input Low Voltage | VIL | | | 0.8 | V | VDD = 5 V |
| Input High Voltage | VIH | 2.0 | | | V | VDD = 5 V |
| Input High Leakage | ILIH | | | +10 | µA | VIN = VDD |
| Input Low Leakage | ILIL | | | -10 | µA | VIN = 0V |
| **$IN_{ts}$ - TTL level input pin Schmitt-trigger input pin** | | | | | | |
| Input Low Threshold | Vt- | 0.5 | 0.8 | 1.1 | V | VDD = 5 V |
| Input High Threshold | Vt+ | 1.6 | 2.0 | 2.4 | V | VDD = 5 V |
| Hysteresis (Vt+ - Vt-) | VTH | 0.5 | 1.2 | | V | VDD = 5 V |
| Input High Leakage | ILIH | | | +10 | µA | VIN = VDD |
| Input Low Leakage | ILIL | | | -10 | µA | VIN = 0V |
| **$IN_c$- CMOS level input pin** | | | | | | |
| Input Low Voltage | VIL | | | 0.3xVD | V | VDD = 5 V |
| Input High Voltage | VIH | 0.7xVD | | | V | VDD = 5 V |
| Input High Leakage | ILIH | | | +10 | µA | VIN = VDD |
| Input Low Leakage | ILIL | | | -10 | µA | VIN = 0V |
| **$IN_{cs}$ - CMOS level schmitt-triggered input pin** | | | | | | |
| Input Low Threshold | Vt- | 1.3 | 1.5 | 1.7 | V | VDD = 5 V |
| Input High Threshold | Vt+ | 3..2 | 3.5 | 3.8 | V | VDD = 5 V |
| Hysteresis (Vt+ - Vt-) | VTH | 1.5 | 2 | | V | VDD = 5 V |
| Input High Leakage | ILIH | | | +10 | µA | VIN = VDD |
| Input Low Leakage | ILIL | | | -10 | µA | VIN = 0V |

## 12.3 AC Characteristics

### 12.3.1 FDC: Data rate = 1 MB/500 KB/300 KB/250 KB/sec.

| PARAMETER | SYM. | TEST CONDITIONS | MIN. | TYP. (NOTE 1) | MAX. | UNIT |
|---|---|---|---|---|---|---|
| SA9-SA0, AEN, $\overline{DACK}$, $\overline{CS}$, setup time to $\overline{IOR}$ ↓ | TAR | | 25 | | | nS |
| SA9-SA0, AEN, $\overline{DACK}$, hold time for $\overline{IOR}$ ↑ | TAR | | 0 | | | nS |
| $\overline{IOR}$ width | TRR | | 80 | | | nS |
| Data access time from $\overline{IOR}$ ↓ | TFD | CL = 100 pf | | | 80 | nS |
| Data hold from $\overline{IOR}$ ↓ | TDH | CL = 100 pf | 10 | | | nS |
| SD to from $\overline{IOR}$ ↑ | TDF | CL = 100 pf | 10 | | 50 | nS |
| IRQ delay from $\overline{IOR}$ ↑ | TRI | | | | 360/570 /675 | nS |
| SA9-SA0, AEN, $\overline{DACK}$, setup time to $\overline{IOW}$ ↓ | TAW | | 25 | | | nS |
| SA9-SA0, AEN, $\overline{DACK}$, hold time for $\overline{IOW}$ ↑ | TWA | | 0 | | | nS |
| $\overline{IOW}$ width | TWW | | 60 | | | nS |
| Data setup time to $\overline{IOW}$ ↑ | TDW | | 60 | | | nS |
| Data hold time from $\overline{IOW}$ ↑ | TWD | | 0 | | | nS |
| IRQ delay from $\overline{IOW}$ ↑ | TWI | | | | 360/570 /675 | nS |
| DRQ cycle time | TMCY | | 27 | | | µS |
| DRQ delay time $\overline{DACK}$ ↓ | TAM | | | | 50 | nS |
| DRQ to $\overline{DACK}$ delay | TMA | | 0 | | | nS |
| $\overline{DACK}$ width | TAA | | 260/430 /510 | | | nS |
| $\overline{IOR}$ delay from $\overline{DRQ}$ | TMR | | 0 | | | nS |
| $\overline{IOW}$ delay from $\overline{DRQ}$ | TMW | | 0 | | | nS |

AC Characteristics, FDC continued

| PARAMETER | SYM. | TEST CONDITIONS | MIN. | TYP. (NOTE 1) | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $\overline{IOW}$ or $\overline{IOR}$ response time from DRQ | TMRW | | | 6/12 /20/24 | | µS |
| TC width | TTC | | 135/220 /260 | | | nS |
| RESET width | TRST | | 1.8/3/3.5 | | | µS |
| $\overline{INDEX}$ width | TIDX | | 0.5/0.9 /1.0 | | | µS |
| $\overline{DIR}$ setup time to $\overline{STEP}$ | TDST | | 1.0/1.6 /2.0 | | | µS |
| $\overline{DIR}$ hold time from $\overline{STEP}$ | TSTD | | 24/40/48 | | | µS |
| $\overline{STEP}$ pulse width | TSTP | | 6.8/11.5 /13.8 | 7/11.7 /14 | 7.2/11.9 /14.2 | µS |
| $\overline{STEP}$ cycle width | TSC | | Note 2 | Note 2 | Note 2 | µS |
| $\overline{WD}$ pulse width | TWDD | | 100/185 /225 | 125/210 /250 | 150/235 /275 | µS |
| Write precompensation | TWPC | | 100/138 /225 | 125/210 /250 | 150/235 /275 | µS |

**Notes:**

1. Typical values for T = 25° C and normal supply voltage.

2. Programmable from 2 mS through 32 mS in 2 mS increments.

### 12.3.2 UART/Parallel Port

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| Delay from Stop to Set Interrupt | TSINT | | 9/16 | | Baud Rate |
| Delay from $\overline{IOR}$ Reset Interrupt | TRINT | 100 pF Loading | | 1 | μS |
| Delay from Initial IRQ Reset to Transmit Start | TIRS | | 1/16 | 8/16 | Baud Rate |
| Delay from $\overline{IOW}$ to Reset interrupt | THR | 100 pF Loading | | 175 | nS |
| Delay from Initial $\overline{IOW}$ to interrupt | TSI | | 9/16 | 16/16 | Baud Rate |
| Delay from Stop to Set Interrupt | TSTI | | | 1/2 | Baud Rate |
| Delay from $\overline{IOR}$ to Reset Interrupt | TIR | 100 pF Loading | | 250 | nS |
| Delay from $\overline{IOR}$ to Output | TMWO | 100 pF Loading | | 200 | nS |
| Set Interrupt Delay from Modem Input | TSIM | | | 250 | nS |
| Reset Interrupt Delay from $\overline{IOR}$ | TRIM | | | 250 | nS |
| Interrupt Active Delay | TIAD | 100 pF Loading | | 25 | nS |
| Interrupt Inactive Delay | TIID | 100 pF Loading | | 30 | nS |
| Baud Divisor | N | 100 pF Loading | | $2^{16}$-1 | |

### 12.3.3 Parallel Port Mode Parameters

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| PD0-7, $\overline{INDEX}$, $\overline{STROBE}$, $\overline{AUTOFD}$ Delay from $\overline{IOW}$ | t1 | | | 100 | nS |
| IRQ Delay from $\overline{ACK}$, nFAULT | t2 | | | 60 | nS |
| IRQ Delay from $\overline{IOW}$ | t3 | | | 105 | nS |
| IRQ Active Low in ECP and EPP Modes | t4 | 200 | | 300 | nS |
| $\overline{ERROR}$ Active to IRQ Active | t5 | | | 105 | nS |

### 12.3.4 EPP Data or Address Read Cycle Timing Parameters

| PARAMETER | SYM. | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Ax Valid to $\overline{IOR}$ Asserted | t1 | 40 | | nS |
| IOCHRDY Deasserted to $\overline{IOR}$ Deasserted | t2 | 0 | | nS |
| $\overline{IOR}$ Deasserted to Ax Valid | t3 | 10 | 10 | nS |
| $\overline{IOR}$ Deasserted to $\overline{IOW}$ or $\overline{IOR}$ Asserted | t4 | 40 | | |
| $\overline{IOR}$ Asserted to IOCHRDY Asserted | t5 | 0 | 24 | nS |
| PD Valid to SD Valid | t6 | 0 | 75 | nS |
| $\overline{IOR}$ Deasserted to SD Hi-Z (Hold Time) | t7 | 0 | 40 | µS |
| SD Valid to IOCHRDY Deasserted | t8 | 0 | 85 | nS |
| $\overline{WAIT}$ Deasserted to IOCHRDY Deasserted | t9 | 60 | 160 | nS |
| PD Hi-Z to PDBIR Set | t10 | 0 | | nS |
| $\overline{WRITE}$ Deasserted to $\overline{IOR}$ Asserted | t13 | 0 | | nS |
| $\overline{WAIT}$ Asserted to $\overline{WRITE}$ Deasserted | t14 | 0 | 185 | nS |
| Deasserted to $\overline{WRITE}$ Modified | t15 | 60 | 190 | nS |
| $\overline{IOR}$ Asserted to PD Hi-Z | t16 | 0 | 50 | nS |
| $\overline{WAIT}$ Asserted to PD Hi-Z | t17 | 60 | 180 | nS |
| Command Asserted to PD Valid | t18 | 0 | | nS |
| Command Deasserted to PD Hi-Z | t19 | 0 | | nS |
| $\overline{WAIT}$ Deasserted to PD Drive | t20 | 60 | 190 | nS |
| $\overline{WRITE}$ Deasserted to Command | t21 | 1 | | nS |
| PBDIR Set to Command | t22 | 0 | 20 | nS |
| PD Hi-Z to Command Asserted | t23 | 0 | 30 | nS |
| Asserted to Command Asserted | t24 | 0 | 195 | nS |
| $\overline{WAIT}$ Deasserted to Command Deasserted | t25 | 60 | 180 | nS |
| Time out | t26 | 10 | 12 | nS |
| PD Valid to $\overline{WAIT}$ Deasserted | t27 | 0 | | nS |
| PD Hi-Z to $\overline{WAIT}$ Deasserted | t28 | 0 | | µS |

### 12.3.5 EPP Data or Address Write Cycle Timing Parameters

| PARAMETER | SYM. | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Ax Valid to $\overline{IOW}$ Asserted | t1 | 40 | | nS |
| SD Valid to Asserted | t2 | 10 | | nS |
| $\overline{IOW}$ Deasserted to Ax Invalid | t3 | 10 | | nS |
| $\overline{WAIT}$ Deasserted to IOCHRDY Deasserted | t4 | 0 | | nS |
| Command Asserted to $\overline{WAIT}$ Deasserted | t5 | 10 | | nS |
| $\overline{IOW}$ Deasserted to $\overline{IOW}$ or $\overline{IOR}$ Asserted | t6 | 40 | | nS |
| IOCHRDY Deasserted to $\overline{IOW}$ Deasserted | t7 | 0 | 24 | nS |
| $\overline{WAIT}$ Asserted to Command Asserted | t8 | 60 | 160 | nS |
| $\overline{IOW}$ Asserted to $\overline{WAIT}$ Asserted | t9 | 0 | 70 | nS |
| PBDIR Low to $\overline{WRITE}$ Asserted | t10 | 0 | | nS |
| $\overline{WAIT}$ Asserted to $\overline{WRITE}$ Asserted | t11 | 60 | 185 | nS |
| $\overline{WAIT}$ Asserted to $\overline{WRITE}$ Change | t12 | 60 | 185 | nS |
| $\overline{IOW}$ Asserted to PD Valid | t13 | 0 | 50 | nS |
| $\overline{WAIT}$ Asserted to PD Invalid | t14 | 0 | | nS |
| PD Invalid to Command Asserted | t15 | 10 | | nS |
| $\overline{IOW}$ to Command Asserted | t16 | 5 | 35 | nS |
| $\overline{WAIT}$ Asserted to Command Asserted | t17 | 60 | 210 | nS |
| $\overline{WAIT}$ Deasserted to Command Deasserted | t18 | 60 | 190 | nS |
| Command Asserted to $\overline{WAIT}$ Deasserted | t19 | 0 | 10 | μS |
| Time out | t20 | 10 | 12 | μS |
| Command Deasserted to $\overline{WAIT}$ Asserted | t21 | 0 | | nS |
| $\overline{IOW}$ Deasserted to $\overline{WRITE}$ Deasserted and PD invalid | t22 | 0 | | nS |

### 12.3.6 Parallel Port FIFO Timing Parameters

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| DATA Valid to nSTROBE Active | t1 | 600 | | nS |
| nSTROBE Active Pulse Width | t2 | 600 | | nS |
| DATA Hold from nSTROBE Inactive | t3 | 450 | | nS |
| BUSY Inactive to PD Inactive | t4 | 80 | | nS |
| BUSY Inactive to nSTROBE Active | t5 | 680 | | nS |
| nSTROBE Active to BUSY Active | t6 | | 500 | nS |

### 12.3.7 ECP Parallel Port Forward Timing Parameters

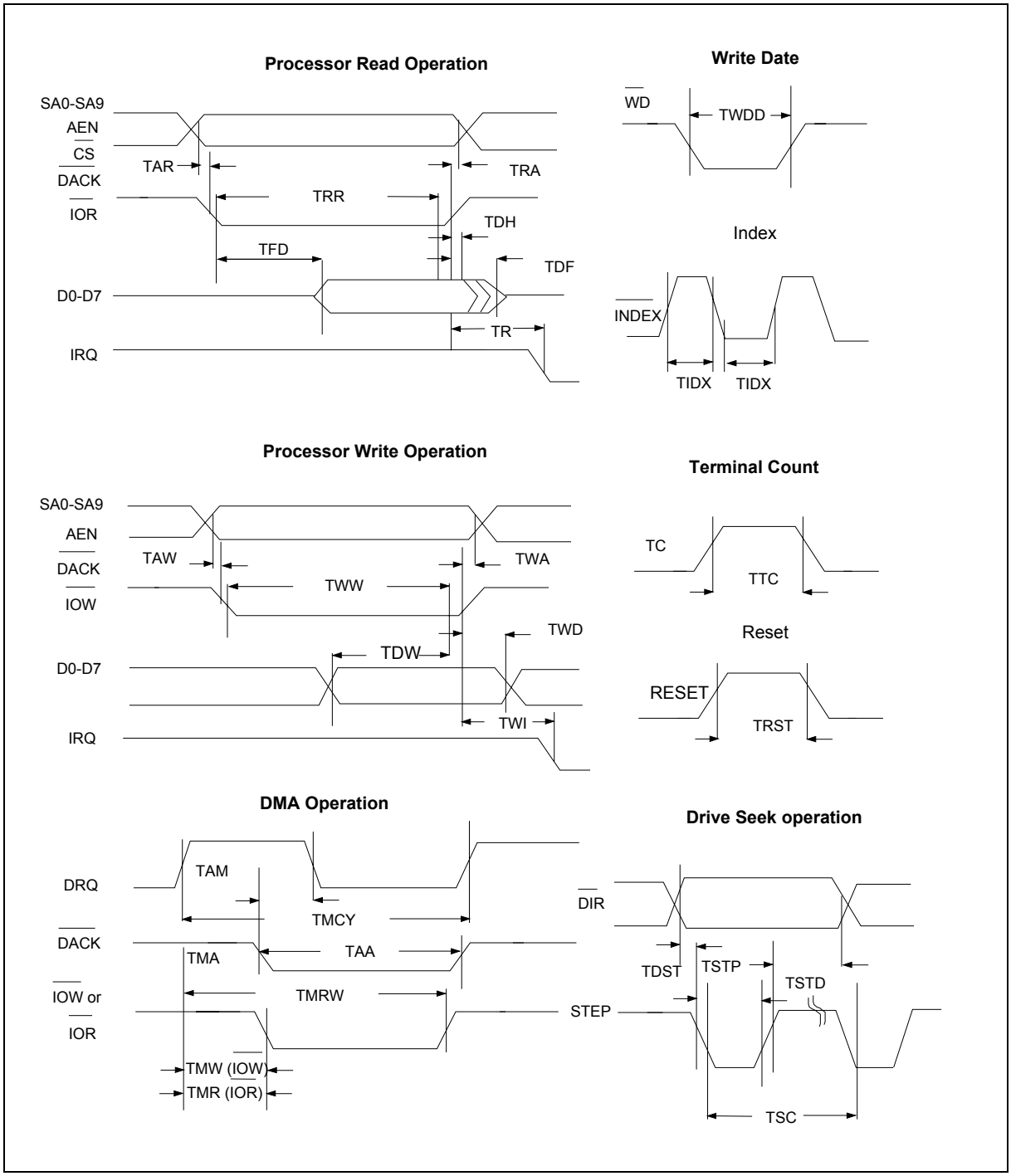
| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| nAUTOFD Valid to nSTROBE Asserted | t1 | 0 | 60 | nS |
| PD Valid to nSTROBE Asserted | t2 | 0 | 60 | nS |
| BUSY Deasserted to nAUTOFD Changed | t3 | 80 | 180 | nS |
| BUSY Deasserted to PD Changed | t4 | 80 | 180 | nS |
| nSTROBE Deasserted to BUSY Deasserted | t5 | 0 | | nS |
| BUSY Deasserted to nSTROBE Asserted | t6 | 80 | 200 | nS |
| nSTROBE Asserted to BUSY Asserted | t7 | 0 | | nS |
| BUSY Asserted to nSTROBE Deasserted | t8 | 80 | 180 | nS |

### 12.3.8 ECP Parallel Port Reverse Timing Parameters

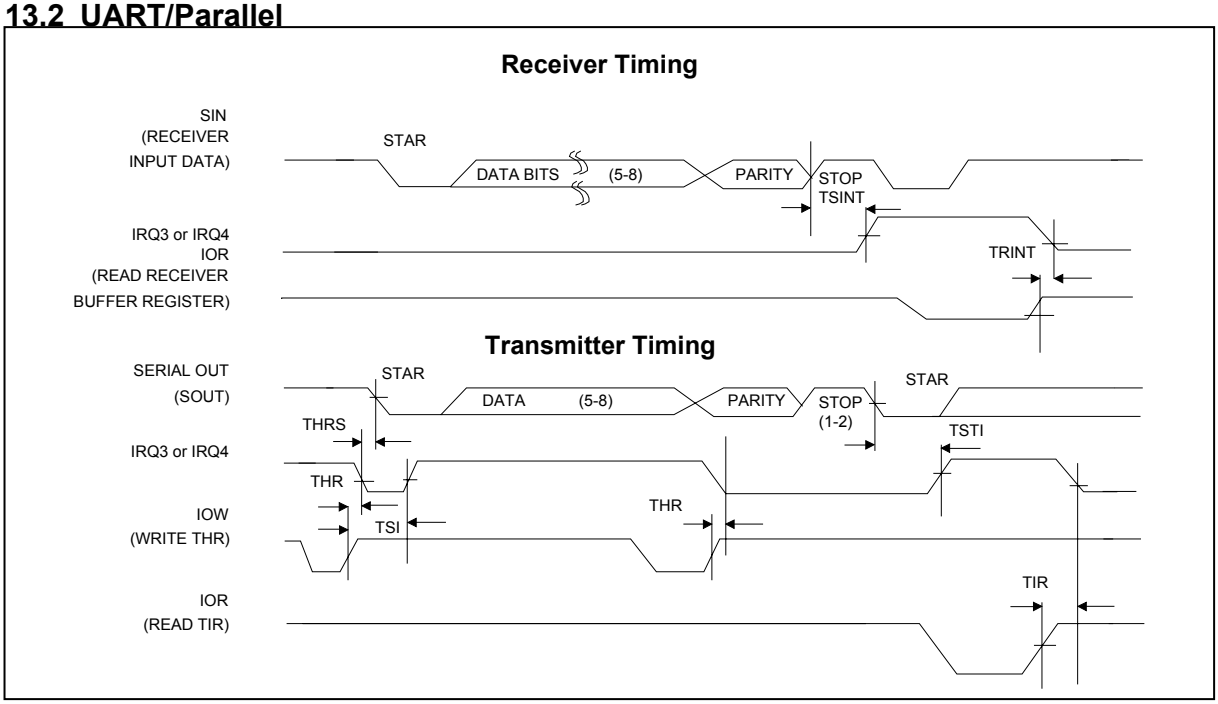
| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| PD Valid to nACK Asserted | t1 | 0 | | nS |
| nAUTOFD Deasserted to PD Changed | t2 | 0 | | nS |
| nAUTOFD Asserted to nACK Asserted | t3 | 0 | | nS |
| nAUTOFD Deasserted to nACK Deasserted | t4 | 0 | | nS |
| nACK Deasserted to nAUTOFD Asserted | t5 | 80 | 200 | nS |
| PD Changed to nAUTOFD Deasserted | t6 | 80 | 200 | nS |

## 13. TIMING WAVEFORMS

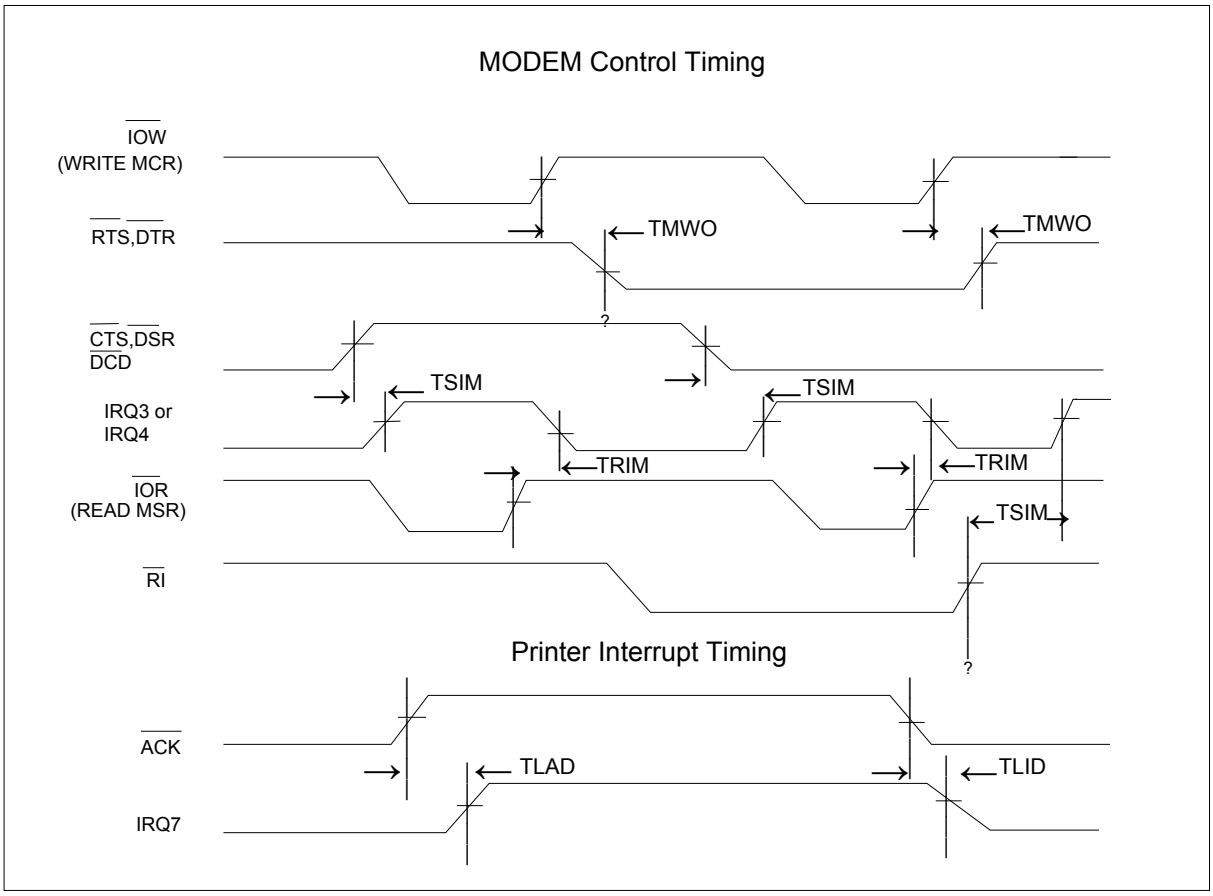
### 13.1 FDC



## 13.2 UART/Parallel

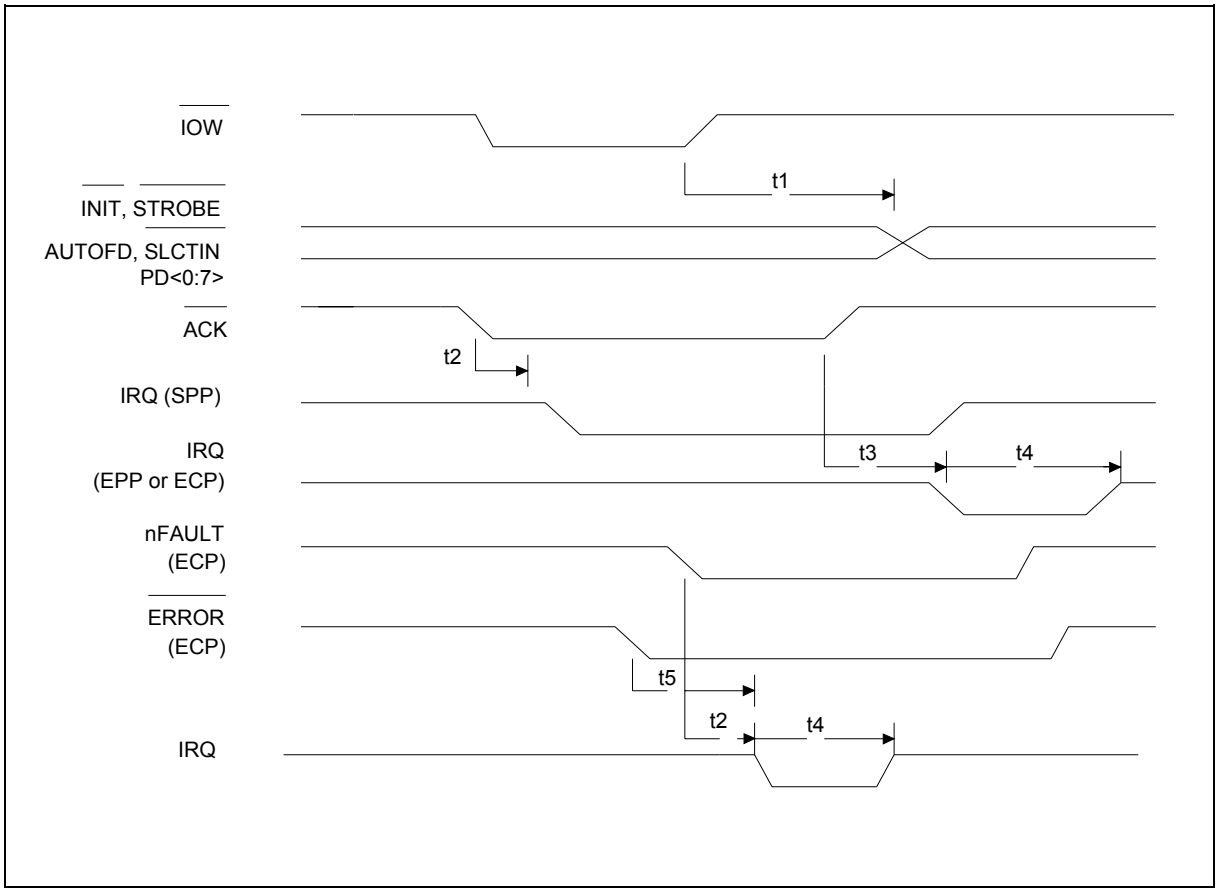


### 13.2.1 Modem Control Timing

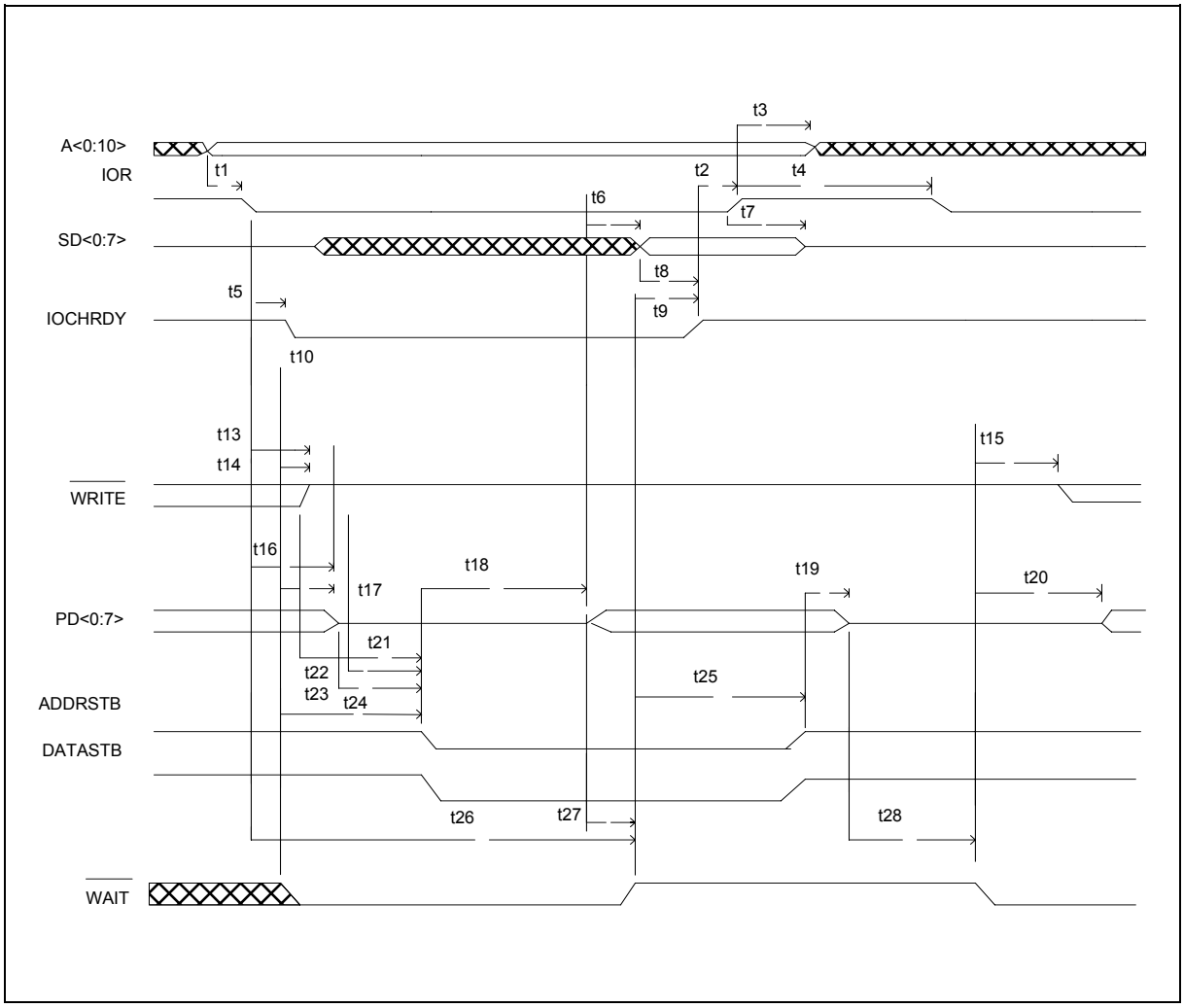


## 13.3 Parallel Port

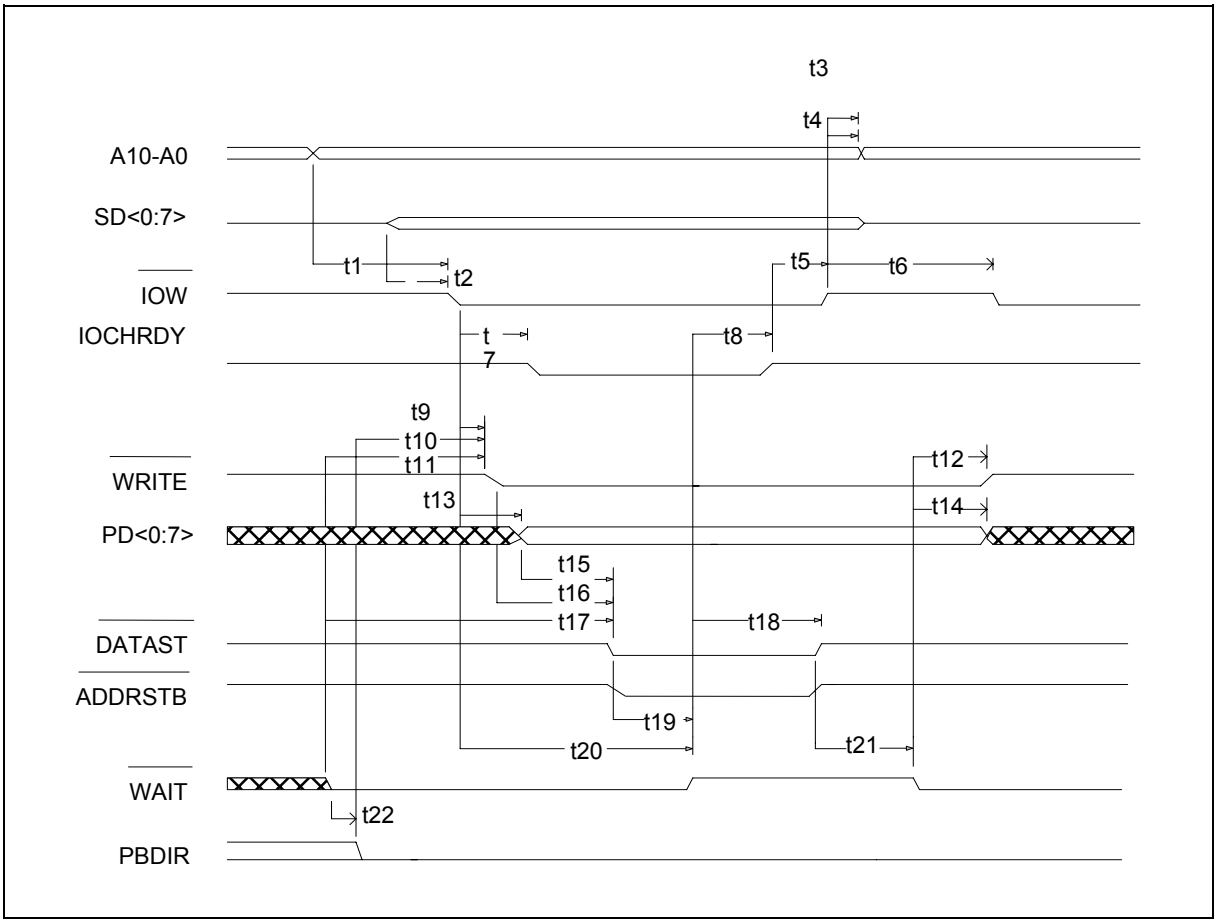
### 13.3.1 Parallel Port Timing



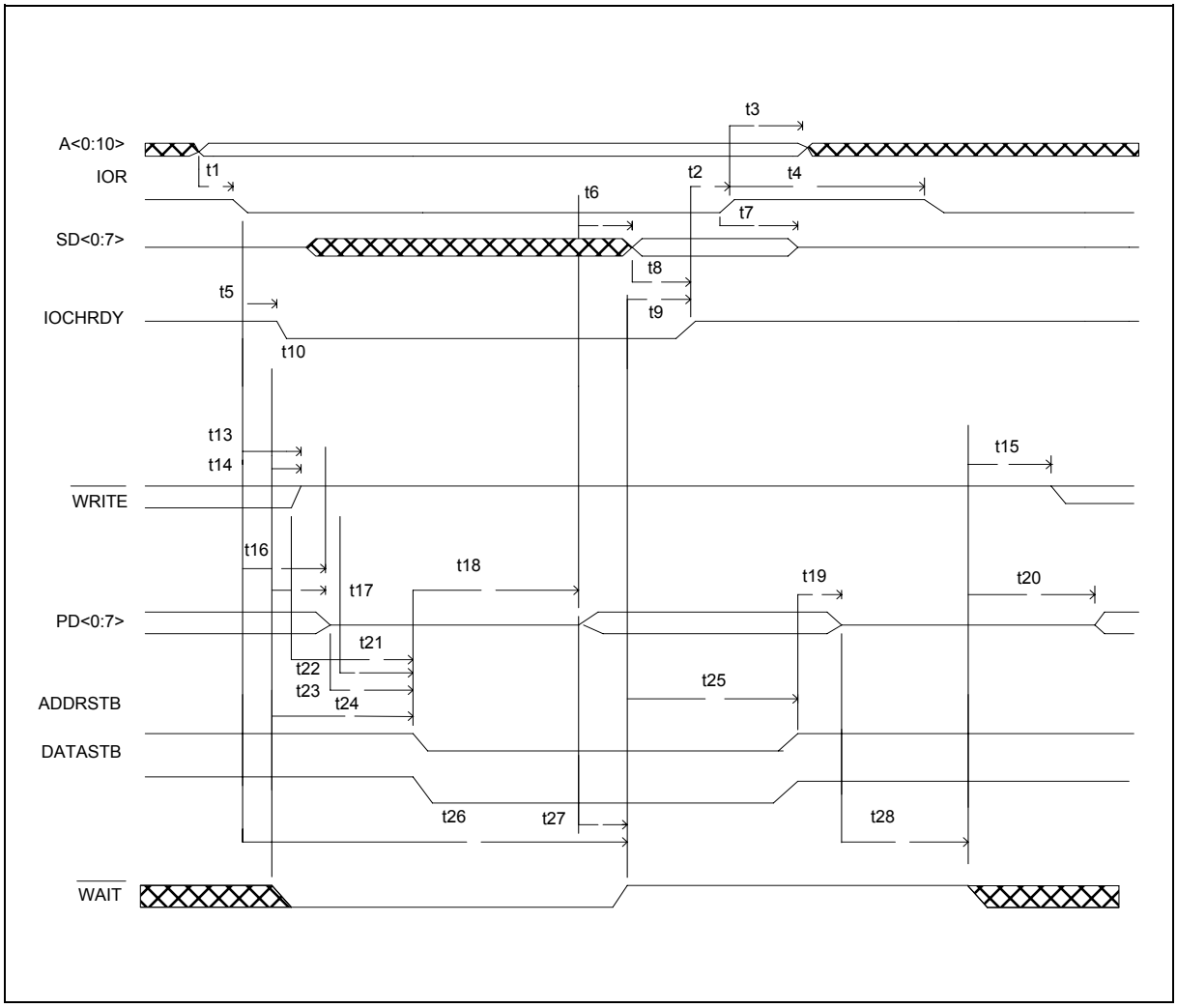
### 13.3.2 EPP Data or Address Read Cycle (EPP Version 1.9)



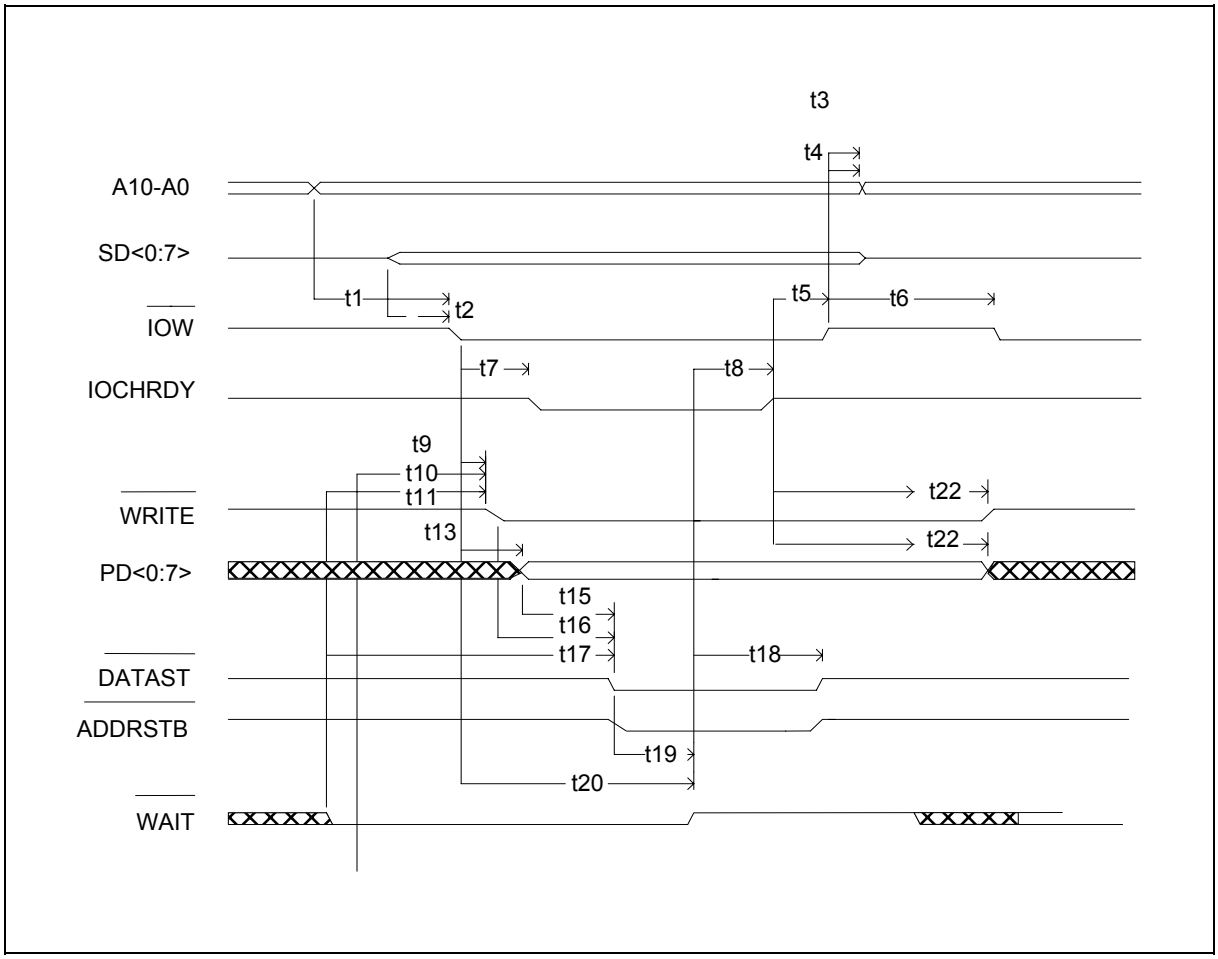
### 13.3.3 EPP Data or Address Write Cycle (EPP Version 1.9)



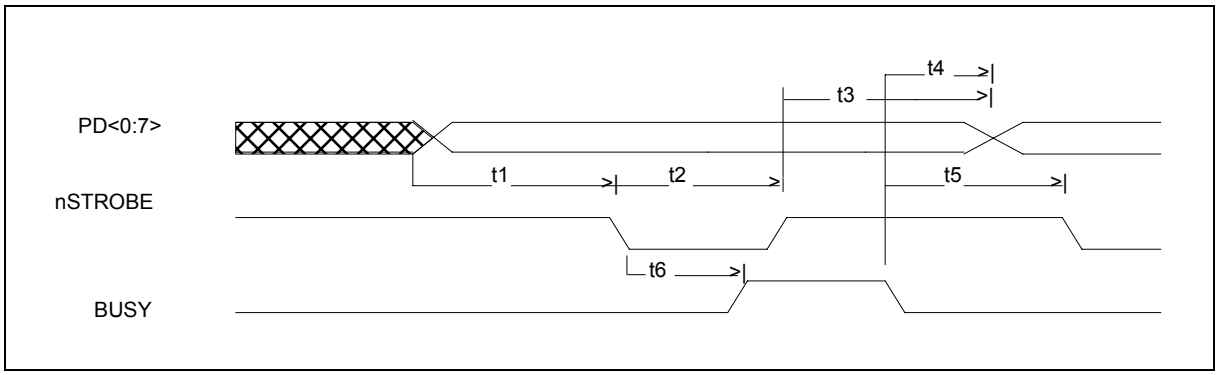
### 13.3.4 EPP Data or Address Read Cycle (EPP Version 1.7)



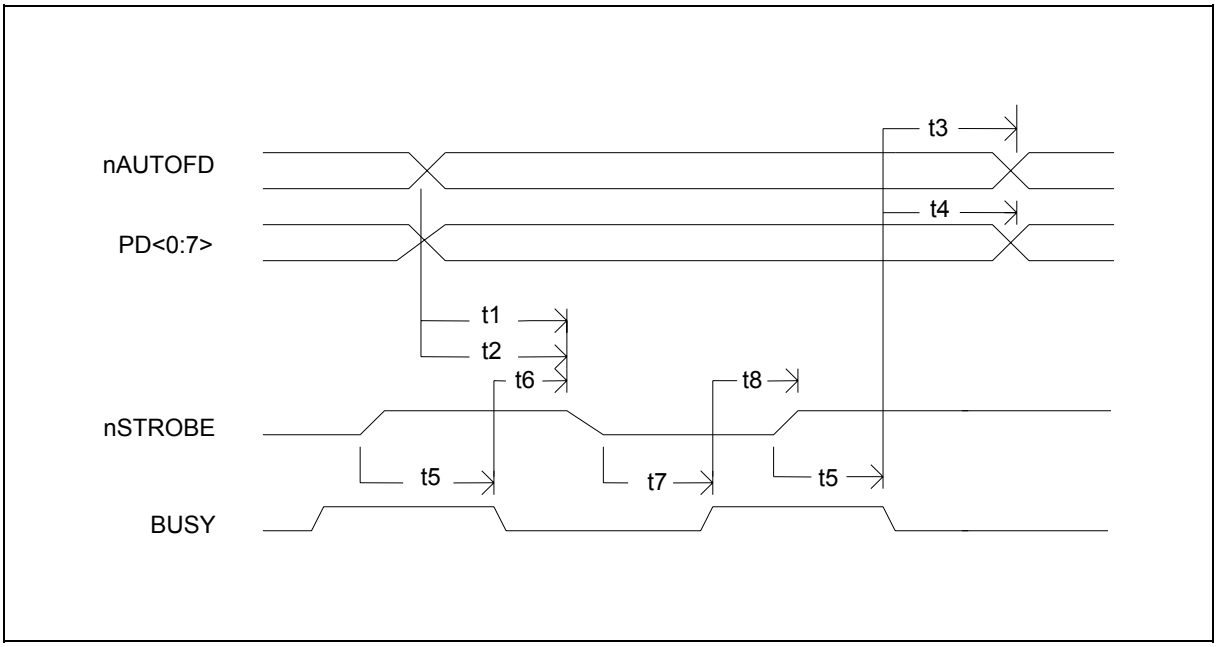
### 13.3.5 EPP Data or Address Write Cycle (EPP Version 1.7)



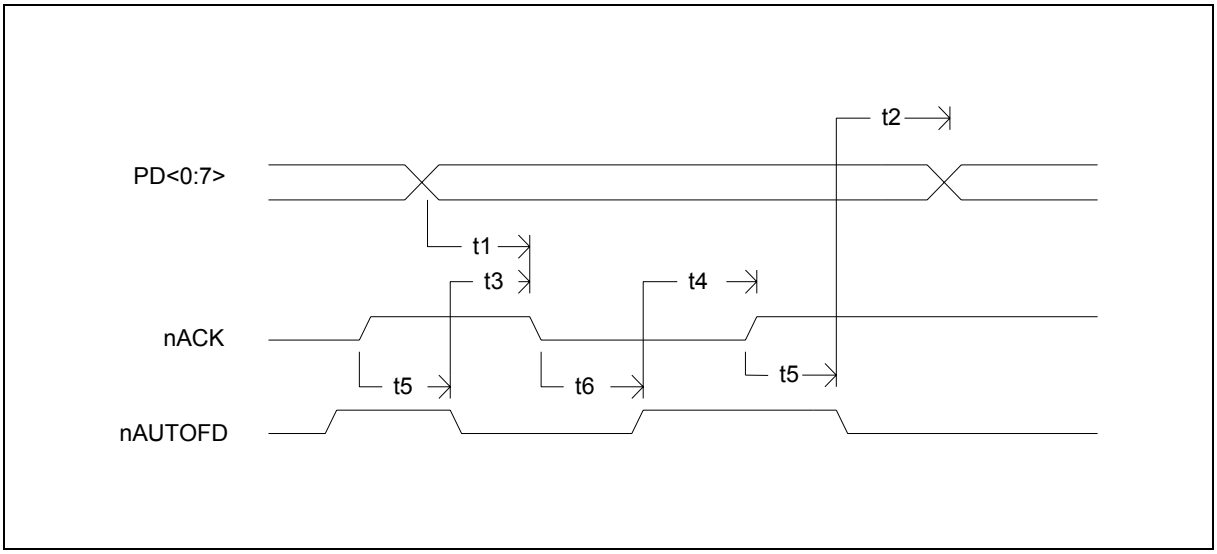

### 13.3.6 Parallel Port FIFO Timing



### 13.3.7 ECP Parallel Port Forward Timing

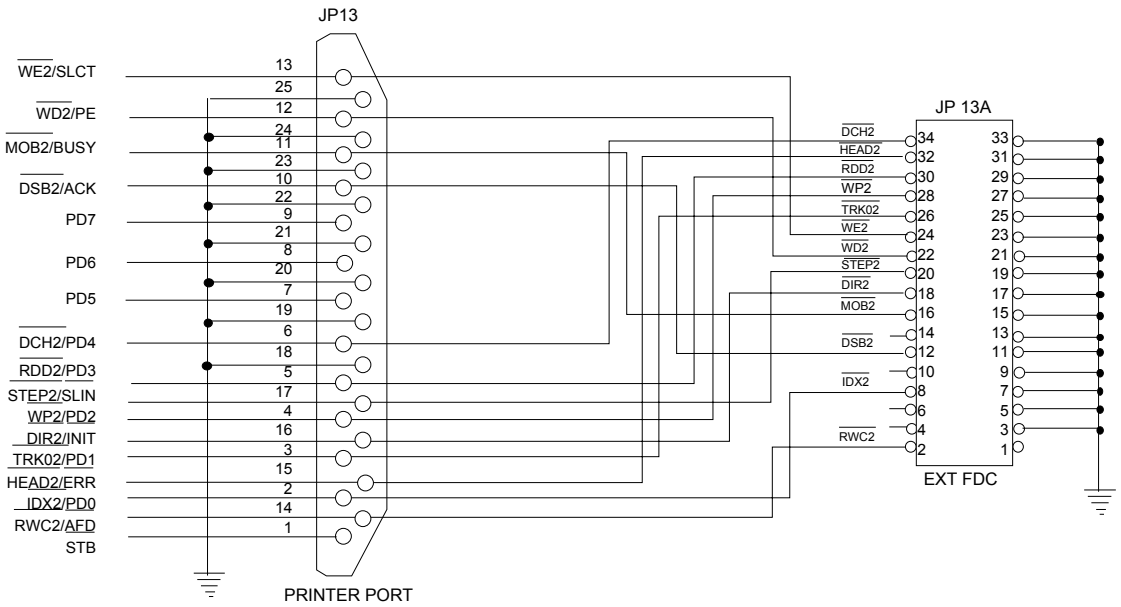



### 13.3.8 ECP Parallel Port Reverse Timing



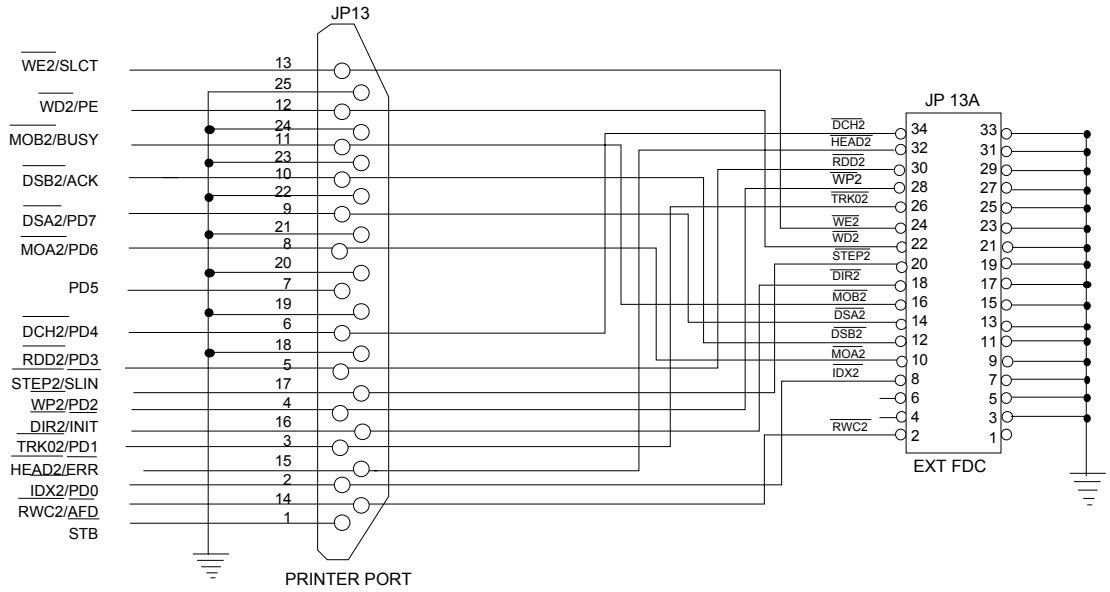
# 14. APPLICATION CIRCUITS

## 14.1 Parallel Port Extension FDD



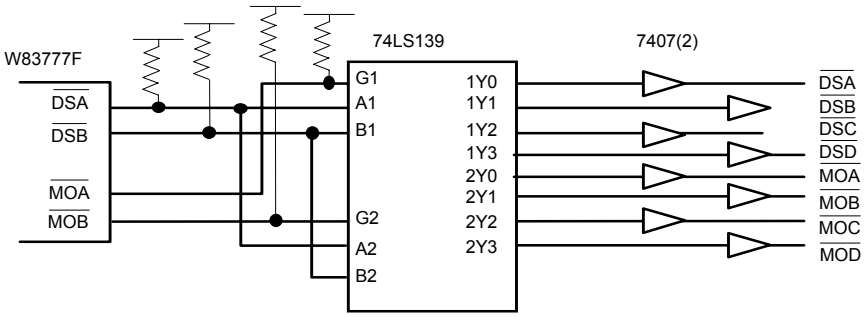

**Parallel Port Extension FDD Mode Connection Diagram**

## 14.2 Parallel Port Extension 2FDD




**Parallel Port Extension 2FDD Connection Diagram**

## 14.3 Four FDD Mode



## 15. ORDERING INFORMATION

| PART NO. | PACKAGE |
|---|---|
| W83877TF | 100-pin QFP |
| W83877TD | 100-pin LQFP |
| W83877TG | 100-pin QFP for lead-free |

## 16. HOW TO READ THE TOP MARKING

Example: The top marking of W83877TF




1st line: Winbond logo

2nd line: the type number: W83877TF

3rd line: tracking code 719 A B 2 7039530

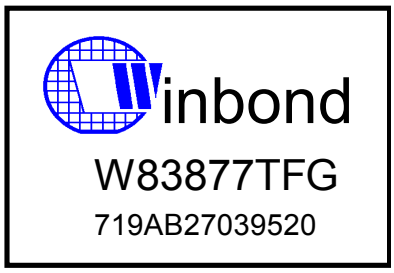
**719**: packages made in '97, week 19

**A**: assembly house ID; A means ASE, S means SPIL....etc

B: IC revision; B means version B, C means version C

**2**: wafers manufactured in Winbond FAB 2

**7039530**: wafer production series lot number




1st line: Winbond logo

2nd line: the type number: W83877TG(Lead-free package)

3rd line: tracking code 719 A B 2 7039530

**719**: packages made in '97, week 19

**A**: assembly house ID; A means ASE, S means SPIL....etc

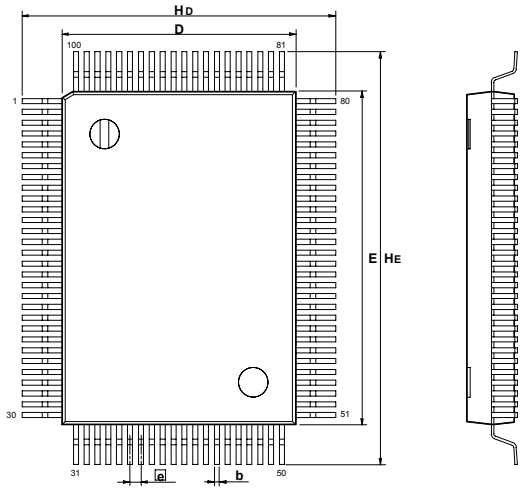
B: IC revision; B means version B, C means version C

**2**: wafers manufactured in Winbond FAB 2

**7039530**: wafer production series lot number

## 17. PACKAGE DIMENSION

### W83877TF (100-pin QFP)

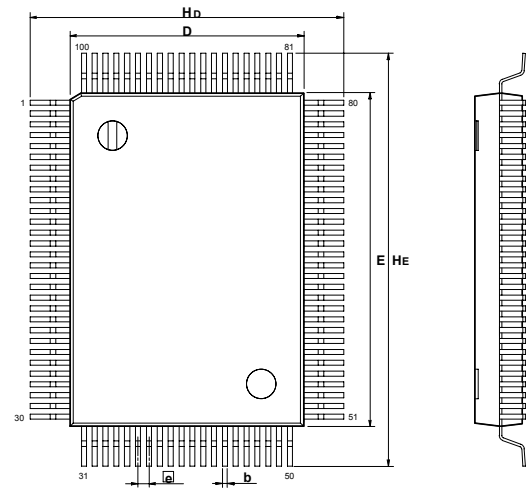


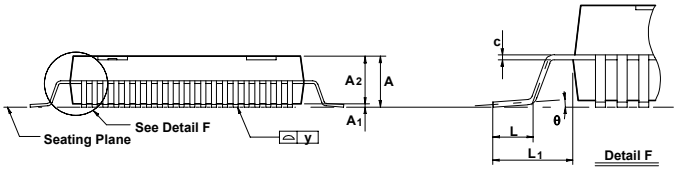

| Symbol | Dimension in inches | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | — | — | 0.130 | — | — | 3.30 |
| $A_1$ | 0.004 | — | — | 0.10 | — | — |
| $A_2$ | 0.107 | 0.112 | 0.117 | 2.73 | 2.85 | 2.97 |
| b | 0.010 | 0.012 | 0.016 | 0.25 | 0.30 | 0.40 |
| c | 0.004 | 0.006 | 0.010 | 0.10 | 0.15 | 0.25 |
| D | 0.546 | 0.551 | 0.556 | 13.87 | 14.00 | 14.13 |
| E | 0.782 | 0.787 | 0.792 | 19.87 | 20.00 | 20.13 |
| e | 0.020 | 0.026 | 0.032 | 0.50 | 0.65 | 0.80 |
| $H_D$ | 0.728 | 0.740 | 0.752 | 18.49 | 18.80 | 19.10 |
| $H_E$ | 0.964 | 0.976 | 0.988 | 24.49 | 24.80 | 25.10 |
| L | 0.039 | 0.047 | 0.055 | 1.00 | 1.20 | 1.40 |
| $L_1$ | 0.087 | 0.094 | 0.103 | 2.21 | 2.40 | 2.62 |
| y | — | — | 0.004 | — | — | 0.10 |
| θ | 0° | — | 12° | 0° | — | 12° |

**Notes:**

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

## W83877TD (100-pin LQFP)




| Symbol | Dimension in inches | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | — | — | — | — | — | — |
| $A_1$ | 0.002 | 0.004 | 0.006 | 0.05 | 0.10 | 0.15 |
| $A_2$ | 0.053 | 0.055 | 0.057 | 1.35 | 1.40 | 1.45 |
| b | 0.009 | 0.013 | 0.015 | 0.22 | 0.32 | 0.38 |
| c | 0.004 | 0.006 | 0.008 | 0.10 | 0.15 | 0.20 |
| D | 0.547 | 0.551 | 0.555 | 13.90 | 14.00 | 14.10 |
| E | 0.783 | 0.787 | 0.791 | 19.90 | 20.00 | 20.10 |
| e | 0.020 | 0.026 | 0.032 | 0.498 | 0.65 | 0.802 |
| $H_D$ | 0.626 | 0.630 | 0.634 | 15.90 | 16.00 | 16.10 |
| $H_E$ | 0.862 | 0.866 | 0.870 | 21.90 | 22.00 | 22.10 |
| L | 0.018 | 0.024 | 0.030 | 0.45 | 0.60 | 0.75 |
| $L_1$ | | 0.039 | | | 1.00 | |
| y | — | — | 0.003 | — | — | 0.08 |
| θ | 0° | — | 7° | 0° | — | 7° |

**Notes:**

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

## Important Notice

**Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.**

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